PCI 9060SD Data Sheet

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REVISION HISTORY

Date	Revision	Comment
11/6/95	0.5	1. New Timing Spec. 2. Added EOT1# (pin 164 on Cx mode, pin 5 on Jx and Sx modes) 3. Added Space 1 (see the New Registers 1Ch, A0h, A4h, A8h and Modified Registers 88h, 8Ch)
5/1/96	0.6	1. Added Subsystem ID and Subsystem Vendor ID, LOC[2Ch] and PCI[2Ch]. 2. Little/Big Endian conversion for DMA transfer. 3. PCI write to Mailbox can generate local interrupt (LINTo#). 4. DMA register offset from PCI side has been changed. 5. Extra EEPROM data can be loaded from EEPROM. 6. Space 1 offset has been changed. 7. PCI Spec. Rev. 2.1 updated (Delayed Read, No Write allowed during Delayed Read, Write Flush). 8. Corrected typographical errors and clarified specifications.
4/17/97	1.0 (PCI 9060 Rev. 1A)	1. Added Timing Diagrams. 2. DMA description on the PCI bus memory is not supported. 3. Vendor and Device ID is not writable. 4. Mailbox interrupts status bits are not supported. 5. Serial EEPROM hold time is changed to 250 ns. 6. BREQo is always driven low (only for PCI 9060 compatibility). 7. Corrected typographical errors and clarified specifications.

1. GENERAL DESCRIPTION

The PCI 9060SD is a PCI bus master interface chip that connects a PCI host bus to three local bus types, selected through mode pins. Each local bus configuration matches the protocol of an Intel 80960 processor, but the PCI 9060SD may be connected to any local bus with a similar design. (Refer to Figure 1-1.)

Table 1-1. Programmable Local Bus Modes

Mode	Description	80960 Processor
Cx	32-bit address / 32-bit data, non-multiplexed	Cx, Hx
Jx	32-bit address / 32-bit data, multiplexed Jx, Kx	Jx, Kx
Sx	32-bit address / 16-bit data, multiplexed Sx	Sx

The PCI 9060SD bus interface chip offers substantial performance advantages over slave adapters or other bus master adapters that rely on the local or host processor to transfer large amounts of data to and from the adapter. The PCI 9060SD provides a bidirectional DMA channel with FIFOs for maximum burst transfers in and out of the adapter. This feature significantly improves overall performance by greatly reducing local or host processor involvement with actual data transfers. The FIFOs ensure data transfers at maximum bus efficiency and burst rates, even while the local bus is operating at a different (and potentially slower) speed than the PCI bus.

Using the PLX PCI 9060SD bus master chip also reduces total hardware and software development costs for disk controller, communication adapter and embedded system designs. The PCI 9060SD provides a single chip interface solution that minimizes board space requirements and ensures PCI hardware compatibility compliance. Because the PCI 9060SD can be used for all intelligent subsystem designs, common driver and initialization software can be used, thus maximizing development resources and increasing the quality of the design.

The PCI 9060SD may be used in three types of adapters; intelligent master, nonintelligent master and target only. In the intelligent master mode, an on-board CPU programs the DMA controller of the 9060SD. If the master is nonintelligent (that is, no CPU), the host system programs the DMA controller of the 9060SD. In the target only mode, the adapter acts purely as a slave to a PCI master. The 9060SD supports Big Endian/Little Endian conversion and programmable prefetch size.
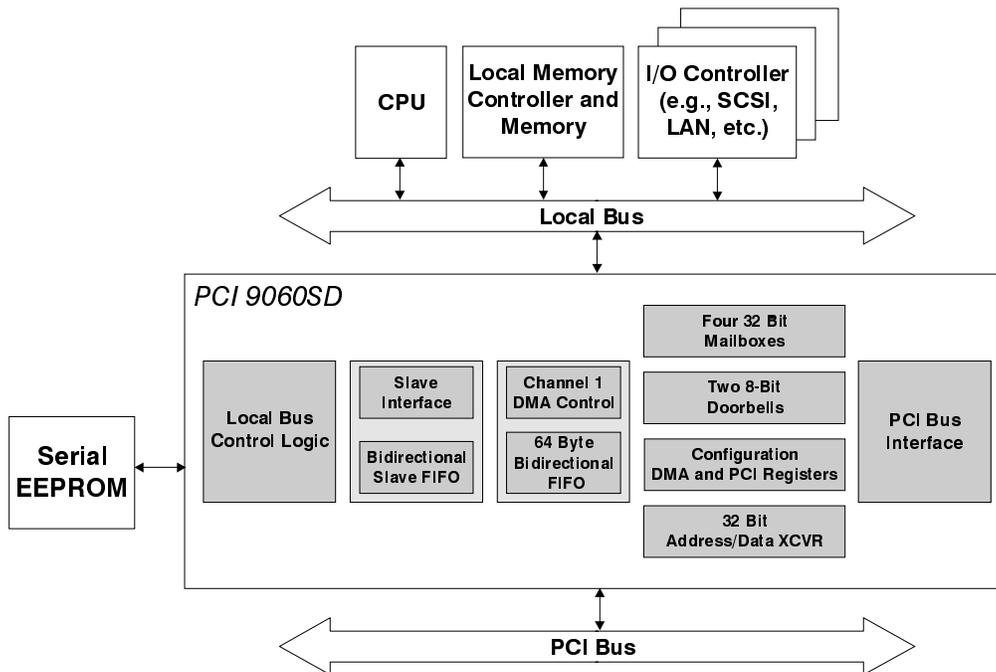
Figure 1-1. Typical Adapter Block Diagram

1.1 MAJOR FEATURES

PCI 9060SD major features include the following:

PCI Specification 2.1 compliant.

Supports Programmable prefetch and Write and Invalidate mode.

Supports chaining from local memory.

PCI ⇔ Local data (DMA) transfers up to 132 MB.

Low-power CMOS in 208 Pin Plastic QFP Package.

Bidirectional DMA controller. Used for bus data transfers between local bus memory and the PCI host**.**

Programmable DMA controller with bidirectional FIFOs. The DMA controller supports both chained and non-chained DMA modes. FIFOs (both are 16 Lwords deep) used for zero wait state burst operation. One is for the DMA controller, the other is for slave interfaces.

Adapter support. PCI Bus Interface supports master (DMA) and slave adapters.

Direct slave. The PCI 9060SD supports both memory mapped and I/O mapped burst accesses to the local bus from the PCI bus. Bidirectional FIFOs enable high-performance bursting on the local and PCI buses.

Big Endian/Little Endian swapping. The PCI 9060SD provides programmable Endian swapping for Direct Slave burst transfers between host and local memory and Local Bus accesses to PCI 9060SD configuration registers.

Exclusive access (LOCK). The PCI 9060SD supports PCI bus interlock ("LOCK#") cycles as a Target.

Interrupt generator. The PCI 9060SD can generate PCI and local interrupts from several sources.

Clock. The PCI 9060SD local bus interface runs from a local TTL clock and generates the necessary internal clocks. This clock can run asynchronously to the PCI clock.

Programmable local bus configurations. The PCI 9060SD supports three bus types—32-bit non-multiplexed (Cx mode), 32-bit multiplexed (Jx mode), and 16-bit multiplexed (Sx mode). The PCI 9060SD operates in one of these three modes, selected through mode pins. May connect directly to Intel i960® Hx, Cx, Jx, Kx, and Sx processors.

Bus drivers. All control, address, and data signals generated by the PCI 9060SD directly drive the PCI bus, without requiring any external drivers.

Serial EEPROM interface. The PCI 9060SD contains an optional serial EEPROM interface that can be used to load configuration information. This is useful for loading information which is unique to a particular adapter (such as Network ID, Vendor ID, and so forth).

Mailbox registers. The PCI 9060SD contains four 32 bit mailbox registers that may be accessed from either the PCI or the local bus.

Doorbell registers. The PCI 9060SD includes two 32 bit doorbell registers. One generates interrupts from the PCI bus to the local bus. The other generates interrupts from the local bus to PCI bus.

Unaligned DMA transfer support. The PCI 9060SD can transfer data on any byte boundary.

1.2 COMPARISON OF PCI 9060 AND PCI 9060SD

Table 1-2. Comparison of PCI 9060 and PCI 9060SD

Feature	PCI 9060	PCI 9060SD
Number of DMA Channel(s)	2 (Ch O, Ch1)	1 (Ch 1)
Number of Local address spaces	2 (Space 0, Expansion ROM)	3 (Space 0, Space 1, and Expansion ROM)
Mailbox Registers	Eight 32 bit	Four 32 bit
Doorbell Registers	Two 32 bit	Two 32 bit
Bidirectional slave FIFO depth	Eight words (16 bytes)	16 Lwords (64 bytes)
LLOCKo# pin for lock cycles	No	Yes
WAITI# pin for wait state generation	No	Yes
BPCLKO pin; buffered PCI clock	No	Yes
DREQ, DACK pins for demand mode DMA support	Yes	Yes (Channel 1 only)
Register addresses	—	Identical, except PCI 9060SD has one DMA register, and Table 4-26 and Table 4-27 were added
Pinout	—	Deleted signals: BREQo (pin 21), DMPAF# (pin 8), DREQ0 (pin 29), DACK0 (pin 30), BTERMo# (pin 28). Added input signals: WAITI# (pin 6), BIGEND# (pin 48) EOT1# (pin 164 IN Cx mode, pin 5 IN Jx and Sx modes) Added output signals: BPCLK (pin 168), LLOCKo# (pin 7)
Big Endian/Little Endian conversion	No	Yes
Spec. 2.1 Deferred Reads	No	Yes
Programmable prefetch counter	No	Yes
Additional Device and Vendor ID register	No	Yes, see (LOC F0h)
All other features (see note)*	Identical	Identical

Note: The PCI 9060SD is software and pin compatible with the PCI 9060. Therefore, designs using the PCI 9060 may be converted to the lower-cost PCI 9060SD with no changes to software or hardware.

2. BUS OPERATION

2.1 PCI BUS CYCLES

The PCI 9060SD is PCI specification 2.1 Compliant.

2.1.1 PCI Target Command Codes

As a target, the PCI 9060SD allows access to the PCI 9060SD internal registers and the local bus using the commands listed in Table 2-1.

Table 2-1. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

All read or write accesses to the PCI 9060SD can be byte, word, or longword accesses. All memory commands are aliased to the basic memory commands. All I/O accesses to the PCI 9060SD are decoded to a longword boundary. The byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

2.1.2 PCI Master Command Codes

The PCI 9060SD can access the PCI bus to perform DMA transfers.

2.1.2.1 DMA Master Command Codes

Table 2-2 lists the memory cycles that can be generated by the PCI 9060SD DMA controllers.

Table 2-2. DMA Master Command Codes

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write & Invalidate	1111 (Fh)

2.2 LOCAL BUS CYCLES

The PCI 9060SD connects a PCI host bus to several local processor bus types—32-bit non-multiplexed (Cx mode), 32-bit multiplexed (Jx mode), and 16-bit multiplexed (Sx mode). The PCI 9060SD operates in one of three modes, selected through mode pins, corresponding to three bus types—Cx, Jx, and Sx.

2.2.1 Local Bus Slave

As a local bus target, the PCI 9060SD allows access to the PCI 9060SD internal registers.

In Cx and Jx modes, local bus slave accesses to the PCI 9060SD must be for a 32 bit nonpipelined bus. In Sx mode, local bus slave accesses to the PCI 9060SD must be for a 16 bit nonpipelined bus.

2.2.2 Local Bus Master

2.2.2.1 Ready/Wait State Control

If the READY input is disabled, the external READY input has no effect on wait states for a local access. Wait states between data cycles are generated internally by a wait state counter. The wait state counter is initialized with its configuration register value at the start of each data access.

If the READY input is enabled, the READY input has no effect until the wait state counter is 0. The READY input then controls the number of additional wait states.

The BTERM input is not sampled until the wait state counter is 0.

2.2.2.2 Burst Mode and Continuous Burst Mode (BTERM "Burst Terminate" Mode)

Burst Mode. If Bursting is enabled and the BTERM input is not enabled, the PCI 9060SD emulates the 80960Sx, 80960Jx or 80960Cx mode of bursting with the exception of the starting burst address. Bursting can start on any boundary and continue up to an address boundary as described below. After the data at the boundary has been transferred, the PCI 9060SD generates a new address cycle (ADS#).

Table 2-3. Burst Mode

Mode	Burst
Cx, Jx	32-bit bus—4 Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
Cx, Jx	16-bit bus—4 words or up to a quad word boundary (LA2, LA1 = 11)
Cx, Jx	8-bit bus—4 bytes or up to a quad byte boundary (LA1, LA0 = 11)
Sx	16-bit bus—8 words or up to a quad Lword boundary (LA3, LA2 = 11)

Continuous Burst Mode (BTERM# "Burst Terminate" mode). BTERM mode enables the PCI 9060SD to perform long bursts to devices that can accept longer than 4 Lword bursts. The PCI 9060SD generates one address cycle and then continues to burst data. If a device requires a new address cycle after a certain address boundary, it can assert BTERM# input to cause the PCI 9060SD to generate a new address cycle. BTERM# input acknowledges the current data transfer and requests that a new address cycle be generated (ADS#). The address will be for the next data transfer. If BTERM mode is enabled, the PCI 9060SD asserts BLAST# only if its FIFOs become FULL/EMPTY or a transfer is complete.

Partial Lword Accesses. Lword accesses in which not all byte enables are asserted are broken into single address and data cycles.

Table 2-4. Partial Lword Accesses

Register Value (PCI 18h)(LOC 98h)		Result
Burst Enable	Bterm Enable	(Number of Transfers)
0	0	Single Cycle (Default)
0	1	Single Cycle
1	0	Burst Mode—burst 4 Lwords at a time (I80960 processor)
1	1	Continuous Burst Mode— burst until BTERM# input (see above descriptions)

2.2.2.3 Recovery States

In Jx and Sx modes, the PCI 9060SD inserts one recovery state between the last data transfer and the next address cycle.

The PCI 9060SD does not support the 80960Jx feature of using the READY input to add recovery states. No additional recovery states are added if the READY input remains asserted during the last data cycle.

2.2.2.4 Local Bus Read Accesses

For all local bus read accesses, the PCI 9060SD reads an entire longword. To a 32 bit local bus the PCI 9060SD performs one read with all byte enables asserted for each Lword. To a 16 bit local bus, the PCI 9060SD performs two 16 bit reads for each Lword. To an 8 bit local bus, the PCI 9060SD performs four 8 bit reads for each Lword.

In other words, for Direct Slave read accesses, the PCI 9060SD reads 4 bytes of data starting at an Lword boundary regardless of the PCI byte enables. For a DMA local bus to PCI bus transfer, the PCI 9060SD reads 4 bytes of data starting at an Lword boundary regardless of the DMA start address and DMA byte count.

2.2.2.5 Local Bus Write Accesses

A byte, word, Lword read mode is programmable through the Local Bus Region Descriptor Register.

For local bus writes, only the bytes specified by a PCI bus master or the PCI 9060SD's DMA controller are written. An access to an 8 or 16 bit bus results in the PCI bus Lword being broken into multiple local bus transfers. For each transfer, the byte enables are encoded as in the 80960Cx to provide local address bits LA[1:0].

2.2.2.6 Direct Slave Write Access to 8- and 16-bit bus

A Direct PCI access to an 8- or 16-bit bus results in the PCI bus Lword being broken into multiple local bus transfers. For each transfer, the byte enables are encoded as in the 80960Cx to provide local address bits LA[1:0].

2.2.2.7 Local Bus Data Parity

There is one data parity pin for each byte lane of the PCI 9060SD data bus (DP[3:0]). Even data parity is generated for each lane during local bus reads from the PCI 9060SD and during PCI 9060SD master writes to the local bus.

Even data parity is checked during local bus writes to the PCI 9060SD and during PCI 9060SD reads from the local bus. Parity is checked for each byte lane with an asserted byte enable. PCHK# is asserted in the clock cycle following the data being checked if a parity error is detected.

Generation or use of local bus data parity is optional. The signals on the data parity pins do not effect operation of the PCI 9060SD. PCI bus parity checking and generation is independent of local bus parity checking and generation.

2.2.2.8 Local Bus Little/Big Endian

The PCI bus is a Little Endian bus. That is, data is longword aligned to the lowermost byte lane. Byte 0 (address 0) appears in AD[7:0], Byte 1 appears in AD[15:8], Byte 2 appears in AD[23:16] and Byte 3 appears in AD[31:24].

The PCI 9060SD local bus can be programmed to operate in Big or Little Endian mode. In Big Endian mode, the PCI 9060SD transposes the data byte lanes. Data is transferred as follows.

32 bit local bus. Data is longword aligned to the upper most byte lane. Byte 0 appears on Local Data [31:24], Byte 1 appears on Local Data [23:16], Byte 2 appears on Local Data [15:8] and Byte 3 appears on Local Data [7:0].

16 bit local bus. For a 16 bit local bus, the PCI 9060SD can be programmed to use the upper or lower word lane. Table 2-5 and Table 2-6 list the byte lanes and burst order.

Table 2-5. Upper Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-6. Lower Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

8 bit local bus. For an 8 bit bus local bus, the PCI 9060SD can be programmed to used the upper or lower byte lane. Table 2-7 and Table 2-8 list the byte lanes and burst order.

Table 2-7. Upper Byte Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
Second Transfer	Byte 1 appears on Local Data [31:24]
Third Transfer	Byte 2 appears on Local Data [31:24]
Fourth Transfer	Byte 3 appears on Local Data [31:24]

Table 2-8. Lower Byte Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

For each of the following transfer types, the PCI 9060SD local bus can be independently programmed to operate in Little Endian or Big Endian mode:

- Local bus accesses to PCI 9060SD configuration registers

- Direct Slave PCI accesses to Local Address Space 0 and Space 1

- Direct Slave PCI accesses to Expansion ROM

- Local bus Direct Master accesses to the PCI bus

For Local bus configuration accesses, an input pin can be used to dynamically change the Endian mode.

3. FUNCTIONAL DESCRIPTION

3.1 RESET

3.1.1 PCI Bus Input RST#

The PCI bus RST# input, causes all PCI bus outputs to float, resets the entire PCI 9060SD and causes the local reset output LRESETo# to be asserted.

3.1.2 Local Bus Input LRESETi#

When asserted, the LRESETi# input resets the local bus portion of the PCI 9060SD, clears all local configuration registers, and causes the LRESETo# output to be asserted.

3.1.3 Local Bus Output LRESETo#

LRESETo# is asserted when PCI bus RST# input is asserted, the LRESETi# input is asserted, or the software reset bit in the Init Control Register is set to a 1.

3.1.4 Software Reset

A host on the PCI bus can set the software reset bit in the Init Control Register to reset the PCI 9060SD and assert the LRESETo# output. The PCI configuration registers will not be reset.

When the software reset bit is set, the PCI 9060SD responds to PCI accesses but not local bus accesses. The PCI 9060SD remains in this reset condition until the PCI host clears the bit.

3.2 PCI 9060SD INITIALIZATION

The PCI 9060SD configuration registers can be programmed by an optional serial EEPROM and/or by a local processor.

EEPROM Initialization

During serial EEPROM initialization, the PCI 9060SD response to PCI target accesses is RETRYs. During serial EEPROM initialization, the PCI 9060SD response to a local processor is to hold off READYo#.

Local Initialization

The PCI 9060SD will issue RETRYs to all PCI accesses until the Local Init Done bit in the Init Control Register is set. The Init Done bit is programmable through local bus configuration accesses. If this bit is not going to be set by

a local processor, then NB# input should be tied low. Holding NB# input low externally forces the Local Init Done bit to 1.

If an EEPROM is not present and the local init status bit is set to "done" by holding the NB# input low, the PCI 9060SD default values are used.

3.3 EEPROM

After reset, the PCI 9060SD attempts to read the EEPROM to determine its presence. An active low start bit indicates the EEPROM is present. Refer to the manufacturer's data sheet for the particular EEPROM being used.

The EEPROM can be read or programmed from the PCI or Local Bus. Bits [27:24] of the EEPROM Control Register controls the PCI 9060SD pins which enable the reading or writing of EEPROM data bits. Refer to the manufacturer's data sheet for the particular EEPROM being used.

The PCI 9060SD has three EEPROM load options:

- **Short Load mode.** SHORT# input pin is pulled down, the PCI 9060SD loads the first 5 Lwords from the EEPROM.

- **Long Load Mode.** SHORT# input pin is pulled up and bit 25 of the "Local Bus Region Descriptor Register [LOC 98h]" is set to a 0, the PCI 9060SD loads the first 17 Lwords from the EEPROM.

- **Extra Long Load Mode.** SHORT# input pin is pulled up and bit 25 of the "Local Bus Region Descriptor Register [LOC 98h]" is set to a 1 during Long Load from the EEPROM, the PCI 9060SD loads the first 21 Lwords from the EEPROM.

3.3.1 Short EEPROM Load

Table 3-1 lists the registers loaded from EEPROM after reset is de-asserted if the SHORT# pin is low.

The bits are organized such that the most significant bit of each 32-bit word is stored first in EEPROM (the first bit in the EEPROM is bit 15 of the Device ID.) The five 32-bit words are stored sequentially in the EEPROM. Therefore, a 256-bit device can be used. (Example: National NM93CS06 or compatible.)

Note: 93C06 is not supported.

Table 3-1. Short EEPROM Load Registers

EEPROM Offset	EEPROM Value	Description
0	906E	Device ID
2	10B5	Vendor ID
4	0680	Class Code
6	0002	Class Code, Revision
8	0000	Maximum Latency, Minimum Grant
A	0100	Interrupt Pin, Interrupt Line Routing
C	xxxx	MSW of Mailbox 0 (User Defined)
E	xxxx	LSW of Mailbox 0 (User Defined)
10	xxxx	MSW of Mailbox 1 (User Defined)
12	xxxx	LSW of Mailbox 1 (User Defined)

3.3.2 Long EEPROM Load

Table 3-2 lists the registers loaded from EEPROM after reset is de-asserted if the SHORT# pin is high. The bits are organized such that the most significant bit of each 16-bit word is stored first in the EEPROM (the first bit in the EEPROM is bit 15 of the Device ID). The EEPROM value can be entered into a DATA I/O programmer in the order shown below. The value shown are examples, and will need to be modified for each particular application. The 34 16-bit words shown above are stored sequentially in the EEPROM. A 1K bit device can be used. (Example: National NM93CS46 or compatible.)

Note: 93CS56 is not supported.

MSW = Most Significant Word (bits [31:16])

LSW = Least Significant Word (bits [15:0])

Table 3-2. Long EEPROM Load Registers

EEPROM Offset	EEPROM Value	Description
0	906D	Device ID.
2	10B5	Vendor ID.
4	0680	Class Code.
6	0002	Class Code, Revision.
8	0000	Maximum Latency, Minimum Grant.
A	0100	Interrupt Pin, Interrupt Line Routing.
C	xxxx	MSW of Mailbox 0 (User Defined).
E	xxxx	LSW of Mailbox 0 (User Defined).
10	xxxx	MSW of Mailbox 1 (User Defined).
12	xxxx	LSW of Mailbox 1 (User Defined).
14	FF00	MSW of Range for PCI to Local Address Space 0 (16 MB).
16	0000	LSW of Range for PCI to Local Address Space 0 (16 MB).
18	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 0.
1A	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 0.
1C	0000	MSW of Local Arbitration Register.
1E	0000	LSW of Local Arbitration Register.
20	0000	MSW of Local Bus Big/Little Endian Descriptor Register.
22	0000	LSW of Local Bus Big/Little Endian Descriptor Register.
24	0000	MSW of Range for PCI to Local Expansion ROM.
26	0000	LSW of Range for PCI to Local Expansion ROM.
28	0000	MSW of Local Base Address (Remap) for PCI to Local Expansion ROM.
2A	0000	LSW of Local Base Address (Remap) for PCI to Local Expansion ROM.
2C	4903	MSW of Bus Region Descriptors for PCI to Local Accesses.
2E	00C3	LSW of Bus Region Descriptors for PCI to Local Accesses.
30	0000	Reserved.
32	0000	Reserved.
34	0000	Reserved.
36	0000	Reserved.
38	0000	Reserved.
3A	0000	Reserved.
3C	0000	Reserved.
3E	0000	Reserved.
40	0000	Reserved.
42	0000	Reserved.

Note: There are 60 unused bytes in the EEPROM which can be used for user defined applications.

3.3.3 Extra Long EEPROM Load

An Extra Long Load mode is provided in 9060SD to load 4 more Lwords from the EEPROM. If bit 25 is set to a 1 in the "Local Bus Region Descriptor [LOC 98h]", the 4 Lword registers listed in Table 3-3 will be loaded in addition to normal Long Load process (see Section 3.3.2). Bit 25 of the "Local Bus Region Descriptor [LOC 98h]" must be set to "1" during Long Load Process.

Table 3-3. Extra Long EEPROM Load Registers

EEPROM Offset	EEPROM Value	Description
44	FF00	MSW of Range for PCI to Local Address Space (16 MB).
46	0000	LSW of Range for PCI to Local Address Space (16 MB).
48	0000	MSW of Local Base Address (Remap) for PCI to Local Address Space 1.
4A	0001	LSW of Local Base Address (Remap) for PCI to Local Address Space 1.
4C	4903	MSW of Bus Region Descriptors (Space 1) for PCI to Local Accesses.
4E	00C3	LSW of Bus Region Descriptors (Space 1) for PCI to Local Accesses.
50	906D	Subsystem ID.
52	10B5	Subsystem Vendor ID.

Note: There are 44 unused bytes in the EEPROM which can be used for user defined applications.

3.3.4 Internal Register Access

The PCI 9060SD chip provides several internal registers allowing for maximum flexibility in bus interface design and performance. Among the register types are

- **PCI Registers** (accessible from PCI bus and local bus)
- **Local Configuration Registers** (accessible from PCI bus and local bus)
- **DMA Registers** (accessible from PCI bus and local bus)
- **Mailbox Registers** (accessible from PCI bus and local bus)
- **Doorbell Registers** (accessible from PCI bus and local bus)

Figure 3-1 shows how these registers are accessed.
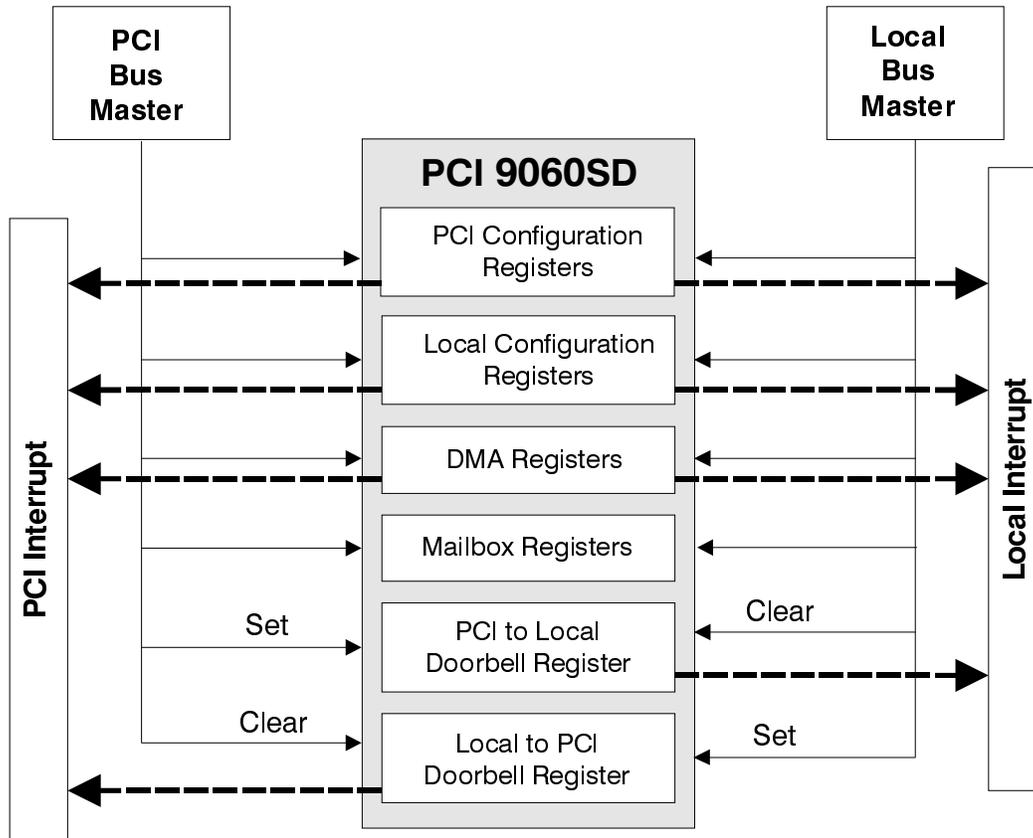
Figure 3-1. PCI 9060SD Internal Register Access

3.3.5 PCI Bus Access to Internal Registers

The PCI 9060SD configuration registers can be accessed from the PCI bus via a configuration type 0 cycle.

The PCI 9060SD internal registers can be accessed via a memory cycle with the PCI bus address matching the base address specified in the PCI 9060SD's PCI Base Address for Memory Mapped Runtime Register or an I/O cycle with the PCI bus address matching the base address specified in the PCI Base Address of the PCI 9060SD for I/O Mapped Runtime Register.

All PCI read or write accesses to the PCI 9060SD registers can be byte, word or longword accesses. All PCI memory accesses to the PCI 9060SD registers can be burst or non-burst. The PCI 9060SD responds with a PCI Disconnect for all I/O accesses to the PCI 9060SD registers.

3.3.6 Local Bus Access to Internal Registers

The local processor can access all the internal registers of the PCI 9060SD through either internal or external address decode logic. The PCI 9060SD provides an Address Decode Mode Pin (ADMODE) that selects whether the internal address decode logic is used or whether the designer will supply an external chip select from an external address decoder. Figure 3-2 shows how the dual address decode logic works.

Address Decode Mode Pin
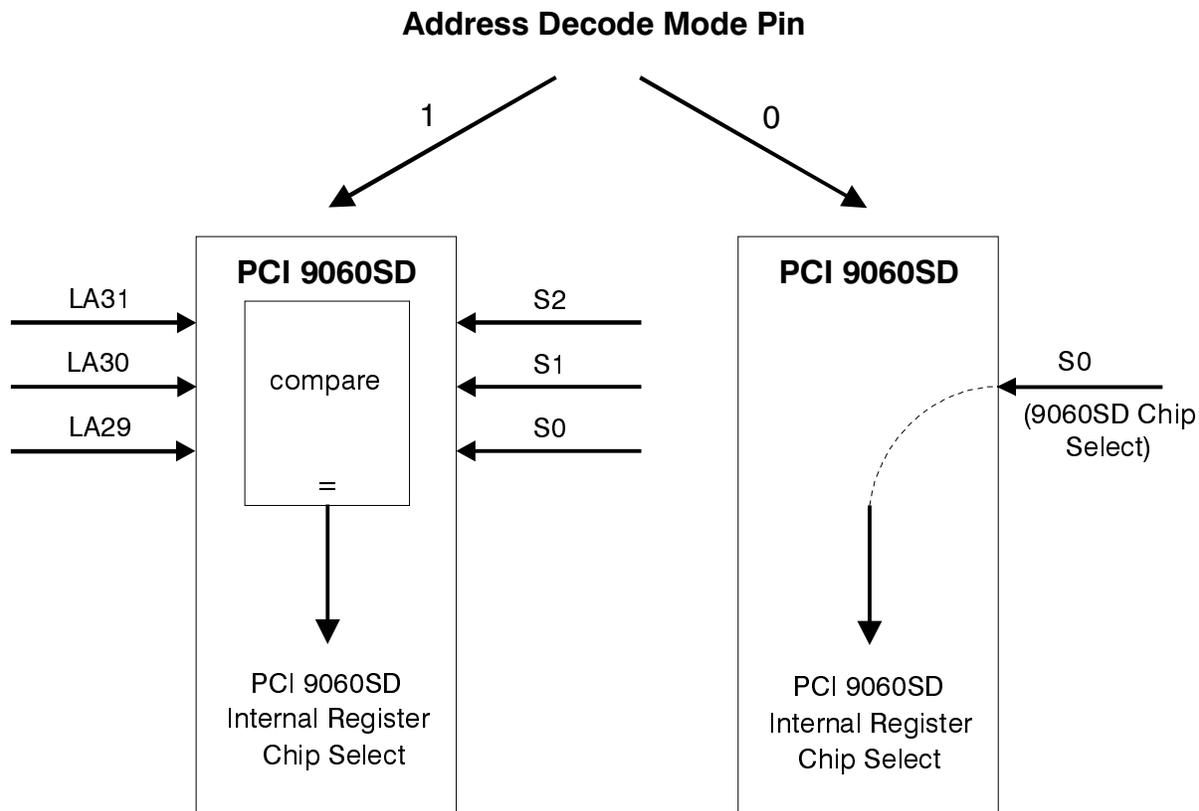
Figure 3-2. Dual Address Decode Mode

If the Address Decode Mode pin is set to 1, the internal PCI 9060SD address decode logic is enabled. In this mode, the PCI 9060SD internal registers are selected when local address bits LA[31:29] match input address select pins S[2:0]. If the Address Decode Mode pin is set to a 0, the PCI 9060SD responds to local bus access when S0 is asserted low through external chip select logic.

Note: S0 must be decoded while ADS# is low.

All local read or write accesses to the PCI 9060SD registers can be byte, word or longword accesses. All local accesses to the PCI 9060SD registers can be burst or non-burst.

For Cx and Jx modes, accesses must be for a 32 bit nonpipelined bus. The PCI 9060SD READYo# indicates a data transfer has completed.

For Sx mode, accesses must be for a 16 bit nonpipelined bus. The PCI 9060SD READYo# indicates a data transfer has completed.

3.4 DIRECT DATA TRANSFER MODES

The PCI host processor can directly access devices on the local bus for reads and writes. Configuration registers within the PCI 9060SD control the decoding and remapping of these accesses to the local address space. Bidirectional FIFOs enable high-performance bursting on the local and PCI bus.

3.4.1 Direct Bus Master Operation

Note: Only supported by PCI 9060 or PCI 9060ES.

3.4.2 Direct Slave Operation (PCI Master to Local Bus Access)

The PCI 9060SD supports both memory mapped burst transfer accesses and I/O mapped single transfer accesses to the local bus from the PCI bus. PCI Base Address registers are provided to set up the adapter's location in PCI memory and I/O space. In addition, local mapping registers are provided to allow address translation from PCI address space to local address space.

The PCI 9060SD disconnects after one transfer for all Direct Slave I/O accesses. For single cycle Direct Slave reads, the PCI 9060SD reads a single local bus Lword. For Direct Slave memory accesses, burst read prefetching can be enabled or disabled through the Local Bus region Descriptor for PCI to Local Accesses Register. If read prefetching is disabled, the PCI 9060SD disconnects after one read transfer. If prefetching is enabled, the read prefetch size can be programmed through the Local Bus Region Description Register.

If the Local side is extremely slow, the PCI 9060SD can be programmed through the Local Arbitration and PCI Mode register to perform delayed reads as specified in PCI specification rev 2.1.

3.4.2.1 PCI to Local Address Mapping

Three local address spaces, space 0, space 1, and expansion ROM, are accessible from the PCI bus. Each space is defined by a set of three registers: Local Address Range, Local Base Address, and PCI Base Address. A fourth register (Bus Region Descriptors for PCI to Local Accesses Register) defines the local bus characteristics for both regions. (Refer to Figure 3-3.)

Each PCI to Local Address space is defined as part of reset initialization as follows.

3.4.2.1.1 Local Bus Initialization Software

Range. Specifies which PCI address bits are to be used to decode a PCI access to Local bus space. Each of the bits corresponds to an address bit with Bit 31 corresponds to Address bit 31. Write "1" to all bits to be included in decode; write "0" to all others.

Remap PCI to Local Addresses into a Local Address space. The bits in this register remap (replace) the PCI address bits used in decode as the Local Address bits.

Local Bus Region Description. Specifies the local bus characteristics.

3.4.2.1.2 PCI Initialization Software

PCI reset software determines how much address space is required by writing a value of all ones (1) to a PCI Base Address register and then reading the value back. The PCI 9060SD return 0s in don't care address bits, effectively specifying the address space required. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register.
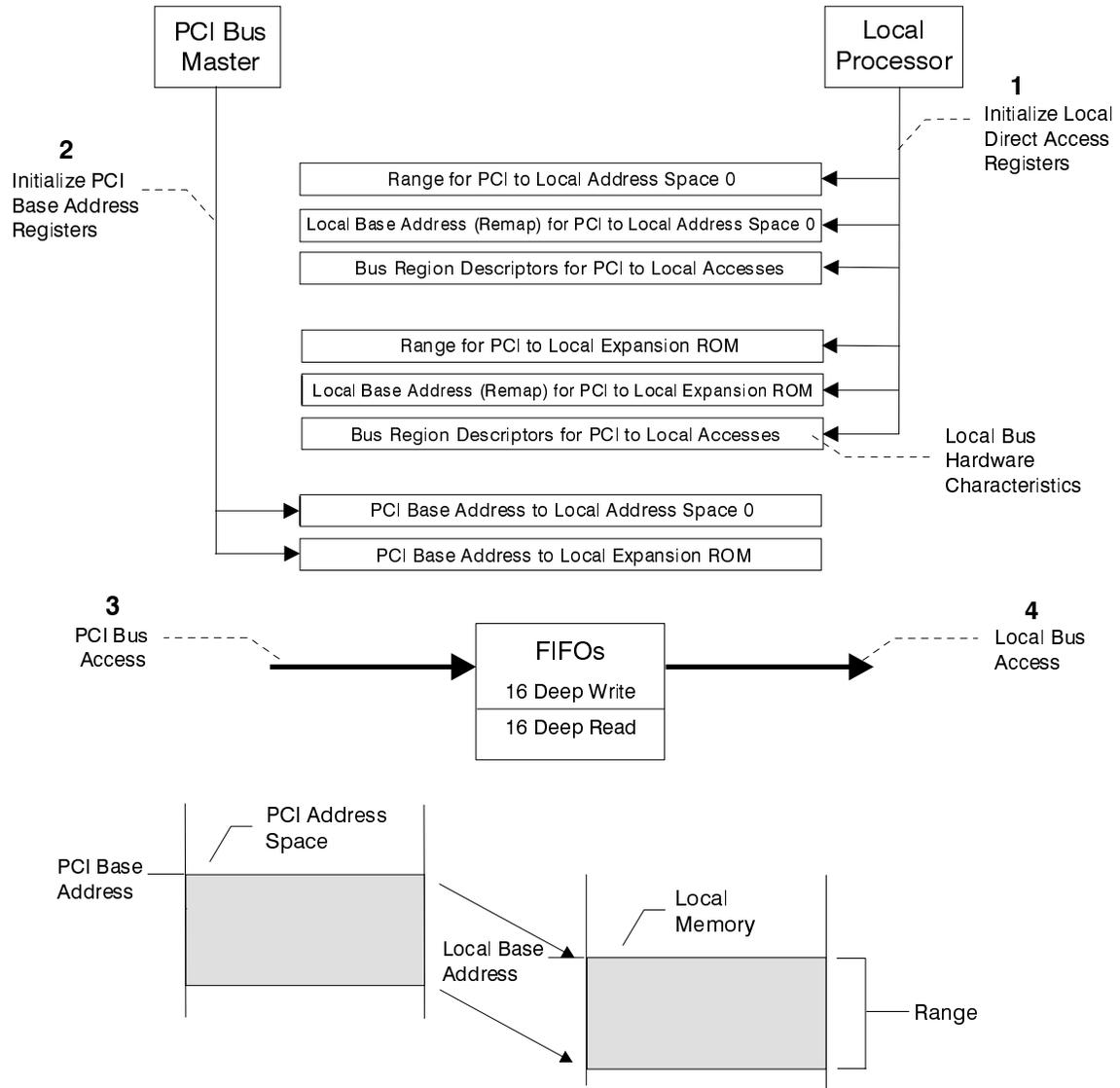
Figure 3-3. Direct Slave Access of Local Bus

Example: A 1 MB local address space 12300000h through 123FFFFFh is accessible from the PCI bus at PCI addresses 78900000h through 789FFFFFh.

1. Local initialization software sets the Range and Local Base address registers as follows:

   - Range—FFF00000h (1 MB, decode the upper 12 PCI address bits)

   - Local Base Address(remap)—123XXXXXh (Local Base Address for PCI to local accesses)

2. PCI Initialization software writes all 1s to the PCI Base Address and then read it back. The PCI 9060SD returns a value FFF00000h. The PCI software then writes to the PCI Base Address register.

   - PCI Base Address—789XXXXXh (PCI Base Address for access to Local Address space)

For PCI direct access to the local bus, the PCI 9060SD has an 16 Lword (64 byte) write FIFO and a 16 Lword read FIFO. The FIFO enables the local bus to operate independent of the PCI bus. The PCI 9060SD can be programmed to return a RETRY response or to throttle TRDY# for any PCI bus transaction that is attempting to write to the PCI 9060SD local bus when the FIFO is full.

For PCI read transactions from the PCI 9060SD local bus, the PCI 9060SD holds off TRDY# while gathering the local bus Lword to be returned. For read accesses mapped to the PCI memory space, the PCI 9060SD prefetches up to 16 Lwords (Programmable) from the local bus. Unused read data is flushed from the FIFO. For read accesses mapped to the PCI I/O space the PCI 9060SD does not prefetch read data, it breaks each read of the burst cycle into a single address/data cycle on the local bus.

The period of time that the PCI 9060SD holds off TRDY# can be programmed in the Local Bus Region Descriptor register. The PCI 9060SD issues a RETRY to the PCI bus transaction master when the programmed time period expires. This would happen when the PCI 9060SD can not gain control of the local bus and return TRDY# within the programmed time period.

3.4.2.2 Direct Slave Lock

The PCI 9060SD supports direct PCI to local bus exclusive accesses (locked atomic operations). A PCI locked operation to local bus results in the entire address space 0, space 1, and expansion ROM space being locked until released by the PCI bus master. The PCI

9060SD asserts LLOCKo# during the first clock of an atomic operation (address cycle) and de-asserts it a minimum of one clock following the last bus access for the atomic operation. LLOCKo# is de-asserted after the PCI 9060SD detects PCI FRAME# and PCI LOCK# de-asserted at the same time. (Refer to Section 8, "Timing Diagrams.") Locked operations are enabled or disabled through the Local Bus Region Descriptor for PCI to Local Accesses Register.

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. For example, if a local master initiates a locked operation, the local arbiter may choose to not grant use of the local bus to other masters until the locked operation is complete.

3.4.3 Direct Slave Priority

Direct Slave accesses have higher priority than DMA accesses.

Direct Slave accesses pre-empt DMA transfers. When the PCI 9060SD DMA controller owns the local bus, its LHOLD output is asserted, its LDSHOLD output is de-asserted and its LHOLDA input is asserted. When a Direct Slave access is made, the PCI 9060SD gives up the local bus within two Lword transfers by de-asserting LHOLD and floating its local bus outputs. After the PCI 9060SD samples its LHOLDA input de-asserted, it requests the local bus for a Direct Slave transfer by asserting LHOLD and LDSHOLD. When the PCI 9060SD receives LHOLDA it drives the bus and performs the Direct Slave transfer. Upon completion of the Direct Slave transfer, the PCI 9060SD gives up the local bus by de-asserting LHOLD, de-asserting LDSHOLD and floating its local bus outputs. After the PCI 9060SD samples its LHOLDA de-asserted and its local pause timer is zero, it requests the local bus for a DMA transfer by re-asserting LHOLD. When it receives LHOLDA it drives the bus and continues with the DMA transfer.

3.5 DMA OPERATION

The PCI 9060SD supports one DMA channel capable of transferring data from the local bus to the PCI bus or from the PCI bus to the local bus. The PCI 9060SD has a programmable DMA controller with bidirectional FIFOs. The DMA controller supports both chained and non-chained DMA modes.

3.5.1 Non-Chaining Mode DMA

The Host Processor or the Local Processor sets the local address, PCI address, transfer count, and transfer direction. The Host or the Local Processor then sets a control bit to initiate the transfer. Once the transfer is complete, the PCI 9060SD generates an interrupt to the local processor (programmable). The local interrupt can be routed to the LINTi# input to generate a PCI interrupt (INTA#).

DMA registers are accessible from the PCI bus and local bus.
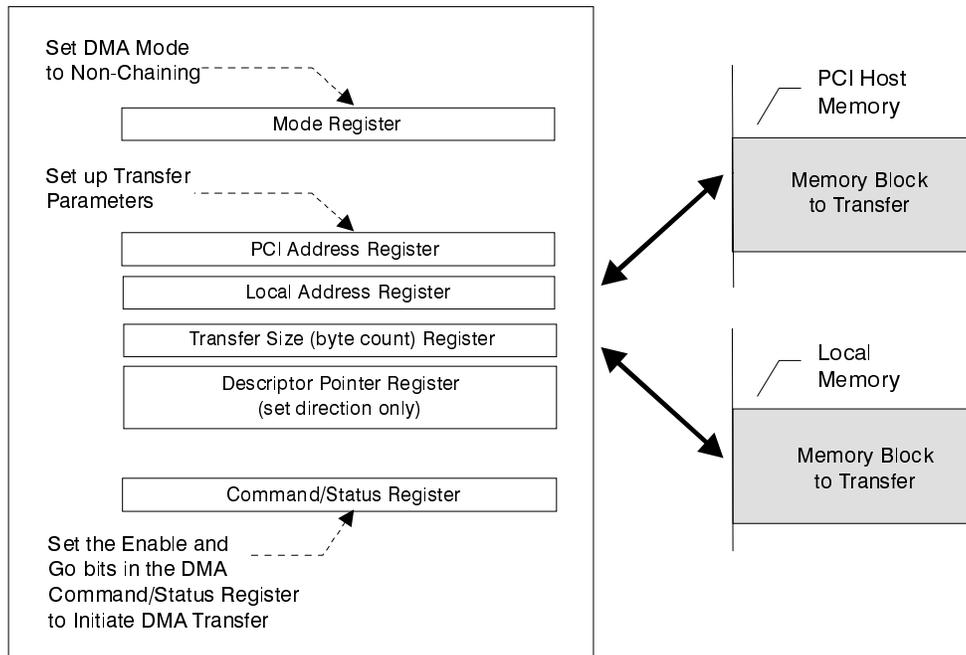
Figure 3-4. Non-Chaining DMA Initialization

3.5.2 Chaining Mode DMA

Chaining DMA operates as follows:

The Host Processor or the Local Processor sets up descriptor blocks in local memory which are composed of a PCI address, Local address, transfer count, transfer direction, and address of the next descriptor block. The Host Processor or the local processor then sets up the address of the initial descriptor block in descriptor pointer register of the PCI 9060SD and initiates the transfer by setting a control bit. The PCI 9060SD loads the first descriptor block and initiates the data transfer. The PCI 9060SD continues to load descriptor blocks and transfer data until it detects the end of chain bit set in the next descriptor pointer register. The PCI 9060SD can be programmed to interrupt the local processor upon completion of each block transfer and after all block transfers have been completed (done). The local interrupt (LINTo#) can be routed to the LINTi# input to generate a PCI interrupt (INTA#).
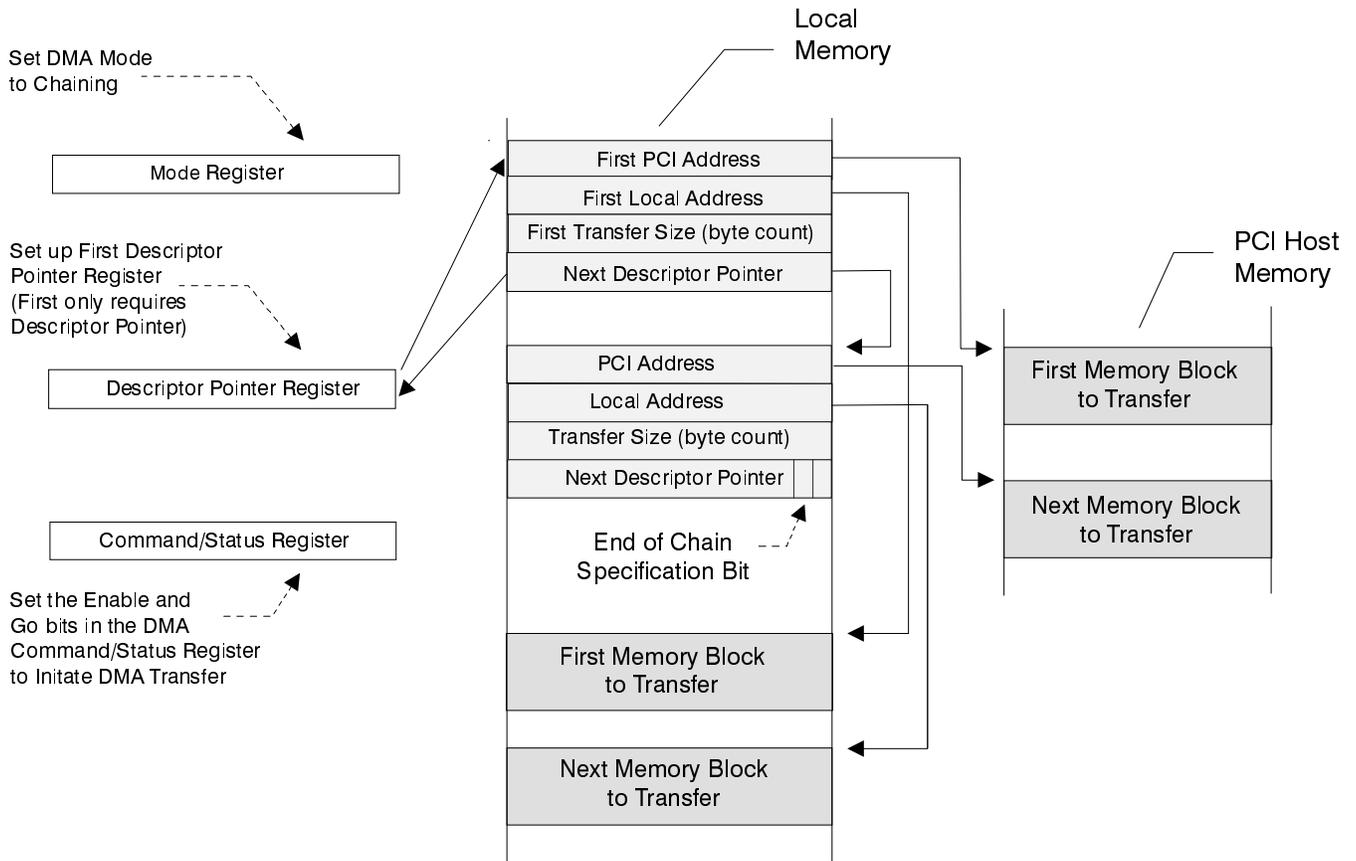
Figure 3-5. Chaining DMA Initialization

3.5.3 DMA Data Transfers

The PCI 9060SD DMA controller can be programmed to transfer data from the PCI bus side to the local bus side or from the local bus side to the PCI bus side. Figure 3-6 and Figure 3-7 provide a description of operation.

3.5.3.1 Local to PCI Bus DMA Transfer

Local Interrupt Generation
(Programmable)
- Done
- Chaining: Terminal
  Count for Current
  Descriptor

Unload FIFO with
PCI Bus
Write Cycles

FIFO

Load FIFO with
Local Bus
Read Cycles

PCI
Arbitration

Local Bus
Arbitration

Chaining Mode Descriptors:

- At the start of each block transfer,
  in Chaining mode only, loads the
  DMA Registers by reading four Lwords
  from the address specified in the Next
  Descriptor Pointer Register.

GNT# REQ# LHOLDA LHOLD

PCI Bus Arbitration:

- Releases control of the PCI bus
  whenever the FIFO becomes empty,
  the PCI latency timer expires and
  PCI GRANT de-asserts, a PCI
  Disconnect is received, or a Direct
  Local to PCI request is pending.

- Rearbitrates for control of the PCI bus
  when the preprogrammed number of
  entries in the FIFO becomes available,
  or after two PCI clocks if a disconnect
  was received.

Local Bus Arbitration:

- Releases control of the local bus whenever
  the FIFO becomes full, terminal count is
  reached, the local latency timer expires,
  the BREQ input is asserted, or a Direct
  PCI to Local Bus request is pending.

- Rearbitrates for control of the local bus
  when the preprogrammed number of
  empty entries in the FIFO becomes
  available. If the latency timer has expired,
  waits until the pause timer expires.

Figure 3-6. Local to PCI Bus DMA Data Transfer Operation

3.5.3.2 PCI to Local Bus DMA Transfer

Load FIFO with
PCI Bus
Read Cycles

FIFO

PCI
Arbitration

Local Bus
Arbitration

Unload FIFO with
Local Bus
Write Cycles

Local Interrupt Generation
(Programmable)
- Done
- Chaining: Terminal
  Count for Current
  Descriptor

Chaining Mode Descriptors:

- At the start of each block transfer,
  in Chaining mode only, loads the
  DMA Registers by reading four Lwords
  from the address specified in the
  Next Descriptor Pointer Register.

GNT# REQ# LHOLDA LHOLD

PCI Bus Arbitration:

- Releases control of the PCI bus
  whenever the FIFO becomes full,
  terminal count is reached, the PCI
  latency timer expires and PCI GRANT
  de-asserts, a PCI Disconnect is received,
  or a Direct Local to PCI request is
  pending.

- Rearbitrates for control of the PCI bus
  when the preprogrammed number of
  empty entries in the FIFO becomes
  available, or after two PCI clocks if a
  disconnect is received.

Local Bus Arbitration:

- Releases control of the local bus whenever
  the FIFO becomes empty, the local latency
  timer expires, the BREQ input is asserted,
  or a Direct PCI to Local Bus request is pending.

- Rearbitrates for control of the local bus
  when the preprogrammed number of
  entries becomes available in the FIFO
  or the PCI terminal count is reached. If the
  latency timer has expired, waits until the
  pause timer expires.

Figure 3-7. PCI to Local Bus DMA Data Transfer Operation

3.5.4 Unaligned Transfers

For unaligned local to PCI transfers, the PCI 9060SD reads a partial Lword from the local bus. It then continues to read Lwords from the local bus. The Lwords are assembled, aligned to the PCI bus address and loaded into the FIFO.

For PCI to local transfers, Lwords are read from the PCI bus and loaded into the FIFO. On the local side, the Lwords are assembled from the FIFO, aligned to the local bus address and written to the local bus. On both the local and PCI buses, the byte enables for writes determine LA0, LA1 for the start of a transfer. For the last transfer the byte enables specify the bytes to be written. All reads are Lwords.

All PCI transfers (reads and writes) are Lwords (32 bits).

3.5.5 Demand Mode DMA

A bit in the configuration Register specifies that the channel operates in Demand Mode. In Demand Mode, the user sets up the DMA controller's configuration registers and initiates a transfer. Data is transferred when the DMA channels DREQ1# input is asserted. It asserts DACK1# to indicate that the current local bus transfer is in response to the DREQ1# input. The DMA controller transfers data until the transfer count is reached. The minimum transfer size per DREQ1# input is one Lword (32 bits). This may result in multiple transfers for an 8- or 16-bit bus. Refer to Section 8, "Timing Diagrams."

3.5.6 DMA Priority

Not Applicable.

3.5.7 DMA Arbitration

The PCI 9060SD DMA controller releases control of the local bus (de-assert LHOLD) once its FIFOs are full in a local to PCI transfer, its FIFOs are empty in a PCI to local transfer, when the local latency timer expires, when the BREQ input is asserted or a Direct Slave access is pending.

The DMA controller releases control of the PCI bus when the FIFOs are full/empty, when the PCI latency timer expires and it loses the PCI grant signal, or a Target Disconnect response is received. It de-asserts its PCI bus request (REQ#) for a minimum of 2 PCI clocks.

3.5.7.1 End Of Transfer (EOT1#) Input

When asserted, current DMA CH1 transfer will terminate regardless of the transfer size.

3.5.7.2 Local Latency and Pause Timers

A local bus latency timer and local bus pause timer are programmable through the DMA Arbitration Register. If the local latency timer expires, the PCI 9060SD completes the current Lword transfer and release LHOLD. After its programmable Pause Timer expires, it reasserts LHOLD. When it receives LHOLDA, it continues with the transfer. The PCI bus transfer continues until the FIFO is empty for a local to PCI transfer or until full for a PCI to local transfer.

3.6 BREQ INPUT

When the PCI 9060SD owns the local bus, its LHOLD output is asserted and its LHOLDA input is asserted by the Local Arbiter. When the PCI 9060SD samples BREQ asserted during a DMA transfer or a Direct Slave write transfer, it gives up the local bus within two Lword transfers by de-asserting LHOLD and floating its local bus outputs. The local arbiter can now grant the local bus to another local master. After the PCI 9060SD samples that its LHOLDA is de-asserted and its local pause timer is zero, it will re-assert LHOLD to request the local bus. When the PCI 9060SD receives LHOLDA it will drive the bus and continue where it left off.

3.7 DOORBELL REGISTERS

There are two 32 bit doorbell interrupt/status registers in the PCI 9060SD. One is assigned to the PCI bus interface, while the other is assigned to the local bus interface.

The local processor can generate a PCI bus interrupt by writing to the PCI doorbell register.

A PCI host can generate a local bus interrupt by writing to the local doorbell register.

3.8 MAILBOX REGISTERS

There are four 32 bit mailbox registers in the PCI 9060SD that can be written and read by both buses. These registers can be used to pass command and status information directly between PCI bus devices and local bus devices.

3.9 INTERRUPTS

3.9.1 PCI Interrupts (INTA#)

The local to PCI doorbell register, local interrupt input, or a master/target abort status condition, can generate a PCI 9060SD PCI Interrupt (INTA#).

INTA# or individual sources of an interrupt can be enabled or disabled through the PCI 9060SD Interrupt Control/Status Register. The Interrupt Control/Status Register also provides interrupt status for each source of the interrupt.

The PCI 9060SD PCI bus interrupt is level output. An interrupt can be cleared by disabling a sources interrupt enable bit or clearing the cause of an interrupt.

3.9.1.1 Local to PCI Doorbell Interrupt

A local bus master can generate a PCI bus interrupt by writing to the Local to PCI Doorbell Register. The PCI host processor can then read the PCI 9060SD Interrupt Control/Status Register to determine that a doorbell interrupt is pending. It can then read the PCI 9060SD Local to PCI Doorbell Register.

Each bit in the Local to PCI Doorbell register is individually controlled. Bits in the Doorbell Register can only be set by the local side. From the local side, writing a 1 to any bit position sets that bit and writing a 0 to a bit position has no effect. Bits in the Local to PCI Doorbell Register can only be cleared from the PCI side. From the PCI side, writing a 1 to any bit position clears that bit and writing a 0 to a bit position has no effect.

The interrupt remains asserted as long as any of the Local to PCI Doorbell Registers bits is set and the PCI Doorbell interrupt is enabled.

When the PCI bus is accessing the Doorbell Register (or any configuration register), the Local bus is held off from accessing the PCI 9060SD registers and the local READYo# signal is de-asserted.

3.9.1.2 Local Interrupt Input

Asserting Local bus input pin LINTi# can generate a PCI bus interrupt. The PCI host processor can read the PCI 9060SD Interrupt Control/Status Register to determine that an interrupt is pending due to the LINTi# pin being asserted.

The interrupt remains asserted as long as the LINTi# pin is asserted and the Local Interrupt input is enabled. Adapter specific action can be taken by the PCI host processor to cause the Local bus to release LINTi#.

3.9.1.3 Master/Target Abort Interrupt

The PCI 9060SD sets the master abort or target abort status bit in the PCI configuration register upon detection of a master or target abort. These status bits cause PCI INTA# to be asserted if interrupts are enabled.

The interrupt remains asserted as long as the master or target abort bits remain set in the PCI Configuration Status Register and master/target abort interrupt is enabled. A PCI type 0 configuration access or a local access must be used to clear the master abort and target abort interrupt bits in the PCI Configuration Status Register.

Bits [26:24] of the Interrupt Control/Status Register are latched at the time of a target abort interrupt or a master abort interrupt. They provide information as to who was master when an abort occurred. They are updated whenever an abort occurs.

3.9.2 Local Interrupts (LINTo#)

A PCI 9060SD Local Interrupt (LINTo#) can be generated by the PCI to Local Doorbell Register access, a PCI BIST interrupt, the DMA Channel 1 done interrupt, the DMA Channel 1 terminal count reached, or the DMA channel 1 abort interrupt.

LINTo# or individual sources of an interrupt can be enabled or disabled through the PCI 9060SD Interrupt Control/Status Register. The Interrupt Control/Status Register also provides interrupt status for each source of the interrupt.

The PCI 9060SD local interrupt is a level output. An interrupt can be cleared by disabling a source's interrupt enable bit or clearing the cause of an interrupt.

3.9.2.1 PCI to Local Doorbell Interrupt

A PCI bus master can generate a local bus interrupt by writing to the PCI to Local Doorbell Register. The local processor can then read the PCI 9060SD Interrupt Control/Status Register to determine that a doorbell interrupt is pending. It can then read the PCI 9060SD PCI to Local Doorbell Register.

Each bit in the PCI to Local Doorbell register is individually controlled. Bits in the Doorbell Register can only be set by the PCI side. From the PCI side, writing a 1 to any bit position sets that bit and writing a 0 to a bit position has no effect. Bits in the PCI to Local Doorbell Register can only be cleared from the Local side. From the Local side, writing a 1 to any bit position clears that bit and writing a 0 to a bit position has no effect.

Note: If local side can not clear the Doorbell Interrupt, do not use the PCI to Local Doorbell Register.

The interrupt remains asserted as long any of the PCI to Local Doorbell Registers bits is set and the Local Doorbell interrupt is enabled.

When the Local bus is accessing the Doorbell Register (or any configuration register), the PCI bus is issued a RETRY.

3.9.2.2 Built-In Self Test Interrupt (BIST)

A PCI bus master can generate a local bus interrupt by performing a PCI type 0 configuration write to a bit in the PCI BIST register. The Local processor can then read the PCI 9060SD Interrupt Control/Status Register to determine that a BIST interrupt is pending.

The interrupt remains asserted as long as the bit is set and the BIST interrupt is enabled. The Local bus should reset the bit when BIST is complete. PCI Host software may fail the device if the bit is not reset after 2 seconds.

3.9.2.3 DMA Channel 1 Interrupt

A DMA channel can generate a local bus interrupt when done (transfer complete) or after a transfer is complete for a descriptor in chaining mode. The Local or PCI processor can then read the PCI 9060SD Interrupt Control/Status Register to determine that a DMA channel's interrupt is pending. A Done Status Bit in the Control/Status Register can be used to determine if the interrupt is a done interrupt or as the result of a transfer for a descriptor in a chain completing.

The Mode Register of a channel is used to enable a done interrupt. In chaining mode, a bit in the Next Descriptor Pointer Register (loaded from local memory) of the channel specifies if an interrupt should be generated at the end of the transfer for the current descriptor.

The interrupt of a channel is cleared by writing 1 to the bit 12 in the DMA Command/Status Register.

3.9.3 PCI SERR# (PCI NMI)

The PCI 9060SD generates an SERR# pulse if parity checking is enabled in the PCI Command Register and it detects an address parity error or the Generate SERR# Bit in the Interrupt Control/Status Register is 0 and a 1 is written.

The SERR# output can be enabled or disabled through the PCI Command Register.

3.9.4 Local LSERR# (Local NMI)

The LSERR# interrupt output is asserted if the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register or a parity error status bit is set in the PCI Status Configuration Register.

If parity error checking is enabled in the PCI Command Register, the PCI 9060SD sets the Master Detected Parity Error Status bit in the PCI Status Register if it detects a parity error during a PCI 9060SD master read or it detects the PCI bus signal PERR# being asserted during a PCI 9060SD master write.

If the PCI 9060SD detects a data parity error during a PCI 9060SD master read, a data parity error during a slave write access to the PCI 9060SD or the PCI 9060SD detects an address parity error, it sets a parity error bit in the PCI Status Register.

The PCI 9060SD Interrupt Control/Status Register can be used to individually enable or disable LSERR# for an abort or parity error. LSERR# is a level output which remains asserted as long as the Abort or Parity Error Status Bits are set.

4. REGISTERS

4.1 REGISTER ADDRESS MAPPING

Table 4-1. PCI Configuration Registers

Local (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9060 family and to ensure compatibility with future enhancements, write "0" to all unused bits.				PCI CFG Register Address
	31 24	23 16	15 8	7 0	
00h	Device ID		Vendor ID		00h
04h	Status		Command		04h
08h	Class Code			Revision ID	08h
0Ch	BIST	Header Type	Latency Timer	Cache Line Size	0Ch
10h	PCI Base Address for Memory Mapped Runtime Registers				10h
14h	PCI Base Address for I/O Mapped Runtime Registers				14h
18h	PCI Base Address for Local Address Space 0				18h
1Ch	PCI Base Address for Local Address Space 1				1Ch
2Ch	Subsystem ID		Subsystem Vendor ID		2Ch
30h	PCI Base Address to Local Expansion ROM				30h
3Ch	Max_lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

Table 4-2. Local Configuration Registers

Local (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9060 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 0	PCI (Offset from Runtime Base Address)
80h	Range for PCI to Local Address Space 0	00h
84h	Local Base Address (Remap) for PCI to Local Address Space 0	04h
88h	Local Arbitration Register	08h
8Ch	Big/Little Endian Descriptor Register	0Ch
90h	Range for PCI to Local Expansion ROM	10h
94h	Local Base Address (Remap) for PCI to Local Expansion ROM	14h
98h	Local Bus Region Descriptors (Space 0 and Expansion ROM) for PCI to Local Accesses	18h
B0h	Range for PCI to Local Address Space 1	30h
B4h	Local Base Address (Remap) for PCI to Local Address Space 1	34h
B8h	Local Bus Region Descriptor (Space 1) for PCI to Local Accesses	38h

Table 4-3. Shared Run Time Registers

Local (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9060 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 0		PCI (Offset from Runtime Base Address)
C0h	Mailbox Register 0		40h
C4h	Mailbox Register 1		44h
C8h	Mailbox Register 2		48h
CCh	Mailbox Register 3		4Ch
E0h	PCI to Local Doorbell Register		60h
E4h	Local to PCI Doorbell Register		64h
E8h	Interrupt Control/Status		68h
ECh	EEPROM Control, PCI Command Codes, User I/O Control, Init Control		6Ch
F0h	Device ID	Vendor ID	70h

Table 4-4. Local DMA Registers

Local (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9060 family and to ensure compatibility with future enhancements, write "0" to all unused bits. 31 0	PCI (Offset from Runtime Base Address)
114h	DMA Ch 1 Mode	94h
118h	DMA Ch 1 PCI Address	98h
11Ch	DMA Ch 1 Local Address	9Ch
120h	DMA Ch 1 Transfer Byte Count	A0h
124h	DMA Ch 1 Descriptor Pointer	A4h
128h	DMA Command/Status Register	A8h
12Ch	DMA Arbitration Register 0	ACh
130h	DMA Arbitration Register 1	B0h

4.2 PCI CONFIGURATION REGISTERS

All registers may be written to or read from in byte, word, or longword accesses.

4.2.1 PCI Configuration ID Register (Offset 00h)

Table 4-5. PCI Configuration ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX (10B5h) if no EEPROM is present and pin NB# (no local bus initialization) is asserted low.	Yes	Local Bus	10B5h
31:16	Device ID. Identifies the particular device. Defaults to the PLX part number for PCI interface chip (9060SD) if no EEPROM is present and pin NB# (no local bus initialization) is asserted low.	Yes	Local Bus	906D

4.2.2 PCI Command Register (Offset 04h)

Table 4-6. PCI Command Register Description

Field	Description	Read	Write	Value after Reset
0	I/O Space. A value of 1 allows the device to respond to I/O space accesses. A value of 0 disables the device from responding to I/O space accesses.	Yes	Yes	0
1	Memory Space. A value of 1 allows the device to respond to memory space accesses. A value of 0 disables the device from responding to memory space accesses.	Yes	Yes	0
2	Master Enable. Controls the ability of a device to act as a master on the PCI bus. A value of 1 allows the device to behave as a bus master. A value of 0 disables the device from generating bus master accesses. State after RST# is 0.	Yes	Yes	0
3	Special Cycle. This bit is not supported.	Yes	No	0
4	Memory Write/Invalidate. (Refer to Table 4-43 for DMA Channel 1 Mode Register (LOC 114h) (PCI 94h), bit 13).	Yes	Yes	0
5	VGA Palette Snoop. This bit is not supported.	Yes	No	0
6	Parity Error Response. A value of 0 indicates a parity error is ignored and operation continues. A value of 1 indicates parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether or not the device does address/data stepping. A value of 0 indicates the device never does stepping. A value of 1 indicates the device always does stepping. This value is hardcoded to 0.	Yes	No	0
8	SERR# Enable. A value of 1 enables the SERR# driver. A value of 0 disables the driver	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates what type of fast back-to-back transfers a Master can perform on the bus. A value of 1 indicates fast back-to-back transfers can occur to any agent on the bus. A value of 0 indicates fast back-to-back transfers can only occur to the same agent as the previous cycle.	Yes	No	0
15:10	Reserved.	Yes	No	0

4.2.3 PCI Status Register (Offset 06h)

Table 4-7. PCI Status Register Description

Field	Description	Read	Write	Value after Reset
6:0	Reserved.	Yes	No	0
7	Fast Back-to-Back Capable. A value of 1 indicates the adapter can accept fast back-to-back transactions. A value of 0 indicates the adapter cannot.	Yes	No	1
8	Master Data Parity Error Detected. This bit is set to a 1 when three conditions are met: 1) the PCI 9060SD asserted PERR# itself or observed PERR# asserted; 2) the PCI 9060SD was the bus master for the operation in which the error occurred; 3) the Parity Error Response bit in the Command Register is set. A value of 1 clears the bit (0).	Yes	Yes	0
10:9	DEVSEL Timing. Indicates timing for DEVSEL# assertion. a value of 01 is medium.	Yes	No	01
11	Target Abort. When this bit is set to a 1, this bit indicates the PCI 9060SD has signaled a target abort. A value of 1 clears the bit (0).	Yes	Yes	0
12	Received Target Abort. A value of 1 indicates the PCI 9060SD has received a target abort signal. A value of 1 clears the bit (0).	Yes	Yes	0
13	Received Master Abort. A value of 1 indicates the PCI 9060SD has received a master abort signal. A value of 1 clears the bit (0).	Yes	Yes	0
14	Signaled System Error. A value of 1 indicates the PCI 9060SD has reported a system error on the SERR# signal. A value of 1 clears the bit (0).	Yes	Yes	0
15	Detected Parity Error. A value of 1 indicates the PCI 9060SD has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command Register is clear). One of three conditions can cause this bit to be set. 1) the PCI 9060SD detected a parity error during a PCI address phase; 2) the PCI 9060SD detected a data parity error when it was the target of a write; 3) the PCI 9060SD detected a data parity error when performing a master read operation. A value of 1 clears the bit (0).	Yes	Yes	0

4.2.4 PCI Revision ID Register (Offset 08h)

Table 4-8. PCI Revision ID Register Description

Field	Description	Read	Write	Value after Reset
7:0	Revision ID. The silicon revision of the PCI 9060SD.	Yes	Local Bus	Current Revision Number

4.2.5 PCI Class Code Register (Offset 09 - 0Bh)

Table 4-9. PCI Class Code Register Description

Field	Description	Read	Write	Value after Reset
7:0	Specific Register Level Programming Interface (00h). No interface defined.	Yes	Local Bus	00
15:8	Subclass Encoding (80h). Other bridge device.	Yes	Local Bus	80h
23:16	Base Class Encoding other Bridge Device.	Yes	Local Bus	06h

4.2.6 PCI Cache Line Size Register (Offset 0Ch)

Table 4-10. PCI Cache Line Size Register Description

Field	Description	Read	Write	Value after Reset
7:0	System cache line size in units of 32-bit words. (Refer to Table 4-43 for DMA Channel 1 Mode Register (LOC 114h) (PCI 94h), bit 13).	Yes	Yes	0

4.2.7 PCI Latency Timer Register (Offset 0Dh)

Table 4-11. PCI Latency Timer Register Description

Field	Description	Read	Write	Value after Reset
7:0	PCI Latency Timer. Specifies in units of PCI bus clocks, the amount of time the PCI 9060SD, as a bus master, can burst data on the PCI bus.	Yes	Yes	0

4.2.8 PCI Header Type Register (Offset 0Eh)

Table 4-12. PCI Header Type Register Description

Field	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies the layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encoding are reserved.	Yes	Local Bus	0
7	Header Type. A value of 1 indicates multiple functions. A value of 0 indicates a single function.	Yes	Local Bus	0

4.2.9 PCI Built-In Self Test (BIST) Register (PCI Offset 0Fh)

Table 4-13. PCI Built-In Self Test (BIST) Register Description

Field	Description	Read	Write	Value after Reset
3:0	A value of 0 indicates the device has passed its test. Nonzero values mean the device failed. Device specific failure codes can be encoded in the nonzero value.	Yes	Local Bus	0
5:4	Reserved, Device returns 0.	Yes	No	0
6	PCI writes a 1 to invoke BIST. Generates an interrupt to local bus. Local bus resets the bit when BIST is complete. Software should fail device if BIST is not complete after 2 seconds. Refer to run time registers for interrupt control/status.	Yes	Yes	0
7	Return 1 if device supports BIST. Return 0 if the device is not BIST compatible.	Yes	Local Bus	0

4.2.10 PCI Base Address Register for Memory Access to Runtime Registers (Offset 10h)

Table 4-14. PCI Base Address Register for Memory Access to Runtime Registers Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates the register maps into Memory space. A value of 1 indicates the register maps into I/O space. *Note: Hardcoded to 0.*	Yes	No	0
2:1	Location of register: 00 - Anywhere in 32 bit memory address space 01 - Below 1 MB memory address space 10 - Anywhere in 64 bit memory address space 11 - Reserved *Note: Hardcoded to 00.*	Yes	No	00
3	Prefetchable. A value of 1 indicates there are no side effects on reads. *Note: Hardcoded to 0.*	Yes	No	0
7:4	Memory Base Address. Memory base address for access to runtime registers. (Minimum Back Size = 128 bytes.) *Note: Hardcoded to 0000.*	Yes	No	0
31:8	Memory Base Address. Memory base address for access to Local Configuration and Shared Run Time registers. (Minimum Back Size = 128 bytes.)	Yes	Yes	0

4.2.11 PCI Base Address Register for I/O Access to Runtime Registers (Offset 14h)

Table 4-15. PCI Base Address Register for I/O Access to Runtime Registers Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. *Note: Hardcoded to 1.*	Yes	No	1
1	Reserved.	Yes	No	0
7:2	I/O Base Address. Base Address for I/O access to runtime registers. (Minimum Block Size = 128 bytes.) *Note: Hardcoded to 0h.*	Yes	No	0
31:8	I/O Base Address. Base Address for I/O access to Local Configuration and Shared Run Time Registers. (Minimum Block Size = 128 bytes.)	Yes	Yes	0

4.2.12 PCI Base Address Register for Memory Access to Local Address Space 0 (Offset 18h)

Table 4-16. PCI Base Address Register for Memory Access to Local Address Space 0 Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Refer to Table 4-24 for Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h).)	Yes	No	0
2:1	Location of register: 00 - Anywhere in 32 bit memory address space 01 - Below 1 MB memory address space 10 - Anywhere in 64 bit memory address space 11 - Reserved (Refer to Table 4-24 for Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h).)	Yes	No	0
3	Prefetchable. A value of 1 indicates there are no side effects on reads. (Refer to Table 4-24 for Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h), bit 3.)	Yes	No	0
31:4	Memory Base Address. Memory base address for access to local address space. (used in conjunction with PCI Configuration Register LOC 80h.)	Yes	Yes	0

4.2.13 PCI Base Address Register for Memory Access to Local Address Space 1 (Offset 1Ch)

Table 4-17. PCI Base Address Register for Memory Access to Local Address Space 1 Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates register maps into Memory space. A value of 1 indicates the register maps into I/O space. (Refer to Table 4-24 for Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h).)	Yes	No	0
2:1	Location of register: 00 - Anywhere in 32 bit memory address space 01 - Below 1 MB memory address space 10 - Anywhere in 64 bit memory address space 11 - Reserved (Refer to Table 4-24 for Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h).)	Yes	No	0
3	Prefetchable. A value of 1 indicates there are no side effects on reads. (Refer to Table 4-24 for Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h), bit 3.)	Yes	No	0
31:4	Memory Base Address. Memory base address for access to local address space (used in conjunction with PCI Configuration Register LOC 80h).	Yes	Yes	0

4.2.14 PCI Configuration ID Register (PCI 2Ch) (LOC 2Ch)

Table 4-18. PCI Configuration ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Subsystem Vendor ID. Identifies the manufacturer of the subsystem device. Defaults to the PCI SIG issued vendor ID of PLX.	Yes	From Serial EEPROM local	10B5h
31:16	Subsystem Device ID. Identifies the particular subsystem device. Defaults to the PLX part number for PCI interface chip (9060SD).	Yes	From Serial EEPROM Local	906D

4.2.15 PCI Expansion ROM Base Register (Offset 30h)

Table 4-19. PCI Expansion ROM Base Register Description

Field	Description	Read	Write	Value after Reset
0	Address Decode Enable. A value of 1 indicates the device accepts accesses to the expansion ROM address. A value of 0 indicates the device does not accept accesses to Expansion ROM space. Should be set to 0 if no Expansion ROM.	Yes	Yes	1
10:1	Reserved.	Yes	No	0
31:11	Expansion ROM Base Address (upper 21 bits).	Yes	Yes	0

4.2.16 PCI Interrupt Line Register (Offset 3Ch)

Table 4-20. PCI Interrupt Line Register Description

Field	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Indicates to which input of the system interrupt controller(s) the device's interrupt line is connected.	Yes	Yes	0

4.2.17 PCI Interrupt Pin Register (Offset 3Dh)

Table 4-21. PCI Interrupt Pin Register Description

Field	Description	Read	Write	Value after Reset
7:0	Interrupt Pin register. Indicates which interrupt pin the device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA#	Yes	Local Bus	1

4.2.18 PCI Min_Gnt Register (Offset 3Eh)

Table 4-22. PCI Min_Gnt Register Description

Field	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Used to specify how long a burst period the device needs assuming a clock rate of 33 MHz. Value is multiple of 1/4 µsec increments.	Yes	Local Bus	0

4.2.19 PCI Max_Lat Register (Offset 3Fh)

Table 4-23. PCI Max_Lat Register Description

Field	Description	Read	Write	Value after Reset
7:0	Max_Lat. Used to specify how often the device needs to gain access to the PCI bus. Value is multiple of 1/4 µsec increments.	Yes	Local Bus	0

4.3 LOCAL CONFIGURATION REGISTERS

4.3.1 Local Address Space 0 Range Register for PCI to Local Bus (PCI 00h) (LOC 80h)

Table 4-24. Local Address Space 0 Range Register for PCI to Local Bus Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates Local address space 0 maps into PCI memory space. A value of 1 indicates address space 0 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: **2/1**　　　　**Meaning** 00　　　Locate anywhere in 32 bit PCI address space 01　　　Locate below 1 MB in PCI address space 10　　　Locate anywhere in 64 bit PCI address space 11　　　Reserved If mapped into I/O space, bit 1 must be a 0. Bit 2 is included with bits [31:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into memory space, a 1 indicates reads are prefetchable. If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.	Yes	Yes	0
31:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 0. Each of the bits corresponds to an address bit. Bit 31 corresponds to Address bit 31. Write "1" to all bits to be included in decode and "0" to all others (used in conjunction with PCI Configuration register 18h). Default is 1 MB.	Yes	Yes	FFF0000h

4.3.2 Local Address Space 0 Local Base Address (Remap) Register for PCI to Local Bus (PCI 04h) (LOC 84h)

Table 4-25. Local Address Space 0 Local Base Address (Remap) Register for PCI to Local Bus Description

Field	Description	Read	Write	Value after Reset
0	Space 0 Enable. A value of 1 enables decoding of PCI addresses for Direct Slave access to local space 0. A value of 0 disables decoding.	Yes	Yes	0
1	Unused.	Yes	No	0
3:2	If local space 0 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits [31:4] for remapping.	Yes	Yes	0
31:4	Remap of PCI Address to Local Address Space 0 into a Local Address Space. The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0

4.3.3 Local Arbitration Register (PCI 08h) (LOC 88h)

Table 4-26. Local Arbitration Register Description

Field	Description	Read	Write	Value after Reset
20:0	These bits are mirrored from/to the DMA Arbitration Register 0 (LOC 12Ch)(PCI ACh).	Yes	Yes	0
21	Local Bus Direct Slave Give up Bus Mode. When set to a 1, the PCI 9060SD de-asserts HOLD and releases the local bus when the Direct Slave write FIFO becomes empty during a Direct Slave write or when the Direct Slave read FIFO becomes full during a Direct Slave read.	Yes	Yes	0
22	Direct Slave LOCK Enable. A value of 1 enables PCI Direct Slave locked sequences. A value of 0 disables Direct Slave locked sequences.	Yes	Yes	0
23	Unused.	Yes	No	0
24	PCI Rev 2.1 Mode. When set to a 1, the PCI 9060SD operates in Delayed Transaction mode for Direct Slave Reads. The PCI 9060SD issues a RETRY and prefetches the read data.	Yes	Yes	0
25	PCI Rev 2.1 No Write Allowed Mode. When set to a 1, the PCI 9060SD will issue a RETRY to any PCI WRITE while the Delayed Read Transaction is pending.	Yes	Yes	0
26	PCI Rev 2.1 Write Flush Mode. When set to a 1, the PCI 9060SD will flush the data from Delayed Read Transaction and perform a Direct Slave Write operation. When the Direct Slave Write is done, perform the Delayed Read Transaction.	Yes	Yes	0
27	Latency Timer enable with BREQ (Bus Request) input. When set to a 1, the PCI 9060SD starts to countdown the Latency Timer before PCI 9060SD de-asserts the LHOLD signal (give up the local bus). When set to a 0, the PCI 9060SD will give up the bus (de-assert the LHOLD signal) after current cycle (usually two local clocks).	Yes	Yes	0
31:28	Unused.	Yes	No	0

4.3.4 Big/Little Endian Descriptor Register (PCI 0Ch) (LOC 8Ch)

Table 4-27. Big/Little Endian Descriptor Register Description

Field	Description	Read	Write	Value after Reset
0	Configuration Register Big Endian Mode. A value of 1 specifies that Big Endian data ordering be used for local accesses to configuration registers. A value of 0 specifies Little Endian ordering. Big Endian mode can be specified for configuration register accesses by asserting input pin BIGEND# during the address phase of the access.	Yes	Yes	0
1	Unused.	Yes	No	0
2	Direct Slave Address Space 0 Big Endian Mode. A value of 1 specifies that Big Endian data ordering be used for Direct Slave accesses to local Address Space 0. A value of 0 specifies Little Endian ordering.	Yes	Yes	0
3	Direct Slave Address Expansion ROM Big Endian select. A value of 1 specifies that Big Endian data ordering be used for Direct Slave accesses to Expansion ROM. A value of 0 specifies Little Endian ordering.	Yes	Yes	0
4	Big Endian byte lane mode. A value of 1 specifies that in Big Endian mode that byte lanes [31:16] be used for a 16 bit local bus and byte lanes [31:24] for an 8 bit local bus. A value of 0 specifies that in Big Endian mode byte lanes [15:0] be used for a 16 bit local bus and byte lane [7:0] for an 8 bit local bus.	Yes	Yes	0
5	Direct Slave Address Space 1 Big Endian mode. A value of 1 specifies that Big Endian data ordering be used for Direct Slave accesses to local Address Space 1. A value of 0 specifies Little Endian ordering.	Yes	Yes	0
6	DMA Channel 1 Big Endian mode. A value of 1 specifies that Big Endian data ordering be used for DMA local Address Space. A value of 0 specifies Little Endian ordering.	Yes	Yes	0
31:7	Unused.	Yes	No	0

4.3.5 Local Expansion ROM Range Register for PCI to Local Bus (PCI 10h) (LOC 90h)

Table 4-28. Local Expansion ROM Range Register for PCI to Local Bus Description

Field	Description	Read	Write	Value after Reset
10:0	Unused.	Yes	No	0
31:11	Specifies which PCI address bits will be used to decode a PCI to local bus expansion ROM. Each of the bits corresponds to an Address bit 31. Write "1" to all bits to be included in decode and "0" to all others (used in conjunction with PCI Configuration register 30h). Default is 64 KB.	Yes	Yes	FFFF00h

4.3.6 Local Expansion ROM Base Address (Remap) Register for PCI to Local Bus (PCI 14h) (LOC 94h)

Table 4-29. Local Expansion ROM Base Address (Remap) Register for PCI to Local Bus Description

Field	Description	Read	Write	Value after Reset
10:0	Unused.	Yes	No	0
31:11	Remap of PCI Expansion ROM space into a Local address space. The bits in this register remap (replace) the PCI address bits used in decode as the local address bits.	Yes	Yes	0

4.3.7 Local Bus Region Descriptor for PCI to Local Accesses Register (PCI 18h) (LOC 98h)

Table 4-30. Local Bus Region Descriptor for PCI to Local Accesses Register Description

Field	Description	Read	Write	Value after Reset
1:0	Memory Space 0 Local Bus Width. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 (Burst mode only) or 11 indicates a bus width of 32 bits (for Cx and Jx modes only).	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
5:2	Memory Space 0 Internal Wait States (data to data).	Yes	Yes	0
6	Memory Space 0 Ready Input Enable. A value of 1 enables Ready input. A value of 0 disables Ready input.	Yes	Yes	0
7	Memory Space 0 Bterm Input Enable. A value of 1 enables Bterm input. A value of 0 disables Bterm input.	Yes	Yes	0
8	Memory Space 0 Prefetch Disable. If mapped into memory space, a 0 enables read prefetching, a value of 1 disables prefetching. If prefetching is disabled, the PCI 9060SD will disconnect after each memory read.	Yes	Yes	0
9	Expansion ROM Space Prefetch Disable. A 0 enables read prefetching, a value of 1 disables prefetching. If prefetching is disabled, the PCI 9060SD will disconnect after each memory read.	Yes	Yes	0
10	Read Prefetch Count Enable. When set to a 1 and memory prefetching is enabled, the PCI 9060SD will prefetch up to the number of Lwords specified in the prefetch count.	Yes	Yes	0
14:11	Read prefetch Counter. When the read Prefetch Count is enabled and memory prefetching is enabled, the PCI 9060SD will prefetch up to the number of Lwords specified in the prefetch counter for memory access to the Memory Space 0 or to the Expansion ROM. After the programmed number of Lwords are read, PCI 9060SD will drop the local bus by de-asserting LHOLD signal. If the counter is set to 0, PCI 9060SD will prefetch 16 Lwords.	Yes	Yes	0
15	Single Read Access Mode Enable. Used in conjunction with Memory Space 0 and Expansion ROM Prefetch Disable. If a PCI read access is made to address space 0 and space 0 Prefetch Disable is set to a 1 or a PCI read access is made to Expansion ROM space and Expansion ROM prefetch Disable is set to a 1, the PCI 9060SD will perform a single read access independent of the PCI bus byte enables. The single access is made as follows: 32 bit local bus = bytes 0, 1, 2, 3 16 bit local bus = bytes 0, 1; bytes 2 and 3 of the PCI Lword are invalid. 8 bit local bus = byte 0; bytes 1, 2, 3 of the PCI Lword are invalid.	Yes	Yes	0
17:16	Expansion ROM Space local device bus width. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 (Burst mode only) or 11 indicates a bus width of 32 bits (for Cx and Jx modes only).	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
21:18	Expansion ROM Space Internal Wait States (data to data).	Yes	Yes	0
22	Expansion ROM Space Ready Input Enable. A value of 1 enables Ready input. A value of 0 disables Ready input.	Yes	Yes	0
23	Expansion ROM Space Bterm Input Enable. A value of 1 enables Bterm input. A value of 0 disables Bterm input.	Yes	Yes	0
24	Memory Space 0 Burst Enable. A value of 1 enables bursting.	Yes	Yes	0
25	Extra Long Load from EEPROM. A value of 1 enables. This value can only be loaded from EEPROM.	Yes	No	0
26	Expansion ROM Space Burst Enable. A value of 1 enables bursting. A value of 0 disables bursting.	Yes	Yes	0

Table 4-30. Local Bus Region Descriptor for PCI to Local Accesses Register Description (continued)

Field	Description	Read	Write	Value after Reset
27	Direct Slave PCI write mode. A value of 0 indicates the PCI 9060SD should disconnect when the Direct Slave write FIFO is full. A 1 indicates the PCI 9060SD should de-assert TRDY# when the write FIFO is full.	Yes	Yes	0
31:28	PCI Target Retry Delay Clocks. Contains the value (multiplied by 8) of the number of PCI bus clocks after receiving a PCI-Local read or write access and not successfully completing a transfer. Only pertains to Direct Slave writes when bit 27 is set to 1.	Yes	Yes	4 (32 clocks)

4.3.8 Local Address Space 1 Range Register for PCI to Local Bus (PCI 30h) (LOC B0h)

Table 4-31. Local Address Space 1 Range Register for PCI to Local Bus Description

Field	Description	Read	Write	Value after Reset
0	Memory space indicator. A value of 0 indicates local address space 1 maps into PCI memory space. A value of 1 indicates address space 1 maps into PCI I/O space.	Yes	Yes	0
2:1	If mapped into memory space, encoding is as follows: **2/1**　　　　　**Meaning** 0 0　　　Locate anywhere in 32 bit PCI address space 0 1　　　Locate below 1 MB in PCI address space 10　　　Locate anywhere in 64 bit PCI address space 1 1　　　Reserved If mapped into I/O space, bit 1 must be a 0. Bit 2 is included with bits [31:3] to indicate decoding range.	Yes	Yes	0
3	If mapped into memory space, a 1 indicates reads are prefetchable. If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.	Yes	Yes	0
31:4	Specifies which PCI address bits will be used to decode a PCI access to local bus space 1. Each of the bits corresponds to an address bit. Bit 31 corresponds to Address bit 31. Write "1" to all bits to be included in decode and "0" to all others (used in conjunction with PCI Configuration register 1Ch). Default is 1 MB.	Yes	Yes	FFF0000h

4.3.9 Local Address Space 1 Local Base Address (Remap) Register for PCI to Local Bus (PCI 34h) (LOC B4h)

Table 4-32. Local Address Space 1 Local Base Address (Remap) Register for PCI to Local Bus Description

Field	Description	Read	Write	Value after Reset
0	Space 1 Enable. A value of 1 enables decoding of PCI addresses for Direct Slave access to local space 1. A value of 0 disables decoding.	Yes	Yes	0
1	Unused.	Yes	No	0
3:2	If local space 1 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits [31:4] for remapping.	Yes	Yes	0
31:4	Remap of PCI Address to Local Address Space 1 into a Local Address Space. The bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.	Yes	Yes	0

4.3.10 Local Bus Region Descriptor for (Space 1) PCI to Local Accesses Register (PCI 38h) (LOC B8h)

Table 4-33. Local Bus Region Descriptor for PCI to Local Accesses Register Description

Field	Description	Read	Write	Value after Reset
1:0	Memory Space 1 Local Bus Width. Programmable for Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 10 or 11 indicates a bus width of 32 bits. The bus width is forced to 16 bits for Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
5:2	Memory Space 1 Internal Wait States (data to data).	Yes	Yes	0
6	Memory Space 1 Ready Input Enable. A value of 1 enables Ready input. A value of 0 disables Ready input.	Yes	Yes	0
7	Memory Space 1 Bterm Input Enable. A value of 1 enables Bterm input. A value of 0 disables Bterm input.	Yes	Yes	0
8	Memory Space 1 Burst Enable. A value of 1 enables bursting. A value of 0 disables bursting.	Yes	Yes	0
9	Memory Space 1 Prefetch Disable. If mapped into memory space, a 0 enables read prefetching, a value of 1 disables prefetching. If prefetching is disabled, the PCI 9060SD will disconnect after each memory read.	Yes	Yes	0
10	Read Prefetch Count Enable. When set to a 1 and memory prefetching is enabled, the PCI 9060SD will prefetch up to the number of Lwords specified in the prefetch count.	Yes	Yes	0
14:11	Read prefetch Count. When set to a 1 and memory prefetching is enabled, the PCI 9060SD will prefetch up to the number of Lwords specified in the prefetch count for memory access to the Memory Space 1.	Yes	Yes	0
15	Single Read Access Mode Enable. Used in conjunction with Memory Space Prefetch Disable. If a PCI read access is made to address Space 1 and Space 1 Prefetch Disable is set to a 1, the PCI 9060SD will perform a single read access independent of the PCI bus byte enables. The single access is made as follows: 32 bit local bus = bytes 0, 1, 2, 3 16 bit local bus = bytes 0, 1 8 bit local bus = byte 0 16 bit local bus, bytes 2, 3 of the PCI Lword will contain invalid data. 8 bit local bus, bytes 1, 2, 3 of the PCI Lword will contain invalid data.	Yes	Yes	0
31:16	Unused.	Yes	No	0

4.4 SHARED RUNTIME REGISTERS

4.4.1 Mailbox Register 0 (PCI 40h) (LOC C0h)

Table 4-34. Mailbox Register 0 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.2 Mailbox Register 1 (PCI 44h) (LOC C4h)

Table 4-35. Mailbox Register 1 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register.	Yes	Yes	0

4.4.3 Mailbox Register 2 (PCI 48h) (LOC C8h)

Table 4-36. Mailbox Register 2 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register.	Yes	Yes	0

4.4.4 Mailbox Register 3 (PCI 4Ch) (LOC CCh)

Table 4-37. Mailbox Register 3 Description

Field	Description	Read	Write	Value after Reset
31:0	32 bit mailbox register	Yes	Yes	0

4.4.5 PCI to Local Doorbell Register (PCI 60h) (LOC E0h)

Table 4-38. PCI to Local Doorbell Register Description

Field	Description	Read	Write	Value after Reset
31:0	Doorbell register. A PCI master can write to this register and it will generate a local interrupt to the local processor. The local processor can then read this register to determine which doorbell bit was asserted. The PCI master sets a doorbell by writing a 1 to a particular bit. The local processor can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes	0

4.4.6 Local to PCI Doorbell Register (PCI 64h) (LOC E4h)

Table 4-39. Local to PCI Doorbell Register Description

Field	Description	Read	Write	Value after Reset
31:0	Doorbell register. The local processor can write to this register and it will generate a PCI interrupt. A PCI master can then read this register to determine which doorbell bit was asserted. The local processor sets a doorbell by writing a 1 to a particular bit. The PCI master can clear a doorbell bit by writing a 1 to that bit position.	Yes	Yes	0

4.4.7 Interrupt Control/Status Register (PCI 68h) (LOC E8h)

Table 4-40. Interrupt Control/Status Register Description

Field	Description	Read	Write	Value after Reset
0	Enable Local bus LSERR#. A value of 1 enables the PCI 9060SD to assert LSERR# interrupt output when the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register.	Yes	Yes	0
1	Enable Local bus LSERR# when a PCI parity error occurs during a PCI 9060SD Master Transfer or a PCI 9060SD Slave access.	Yes	Yes	0
2	Generate PCI bus SERR#. When set to 0, writing a 1 generates a PCI bus SERR#.	Yes	Yes	0
7:3	Unused.	Yes	No	0
8	PCI interrupt enable. A value of 1 enables PCI interrupts.	Yes	Yes	1
9	PCI doorbell interrupt enable. A value of 1 enables doorbell interrupts. Used in conjunction with PCI interrupt enable. Clearing the doorbell interrupt bits causing the interrupt will clear the interrupt.	Yes	Yes	0
10	PCI Abort interrupt enable. A value of 1 enables a master abort or master detect of a target abort to generate a PCI interrupt. Used in conjunction with PCI interrupt enable. Clearing the abort status bits will clear the PCI interrupt.	Yes	Yes	0
11	PCI local interrupt enable. A value of 1 enables a local interrupt input to generate a PCI interrupt. Use in conjunction with PCI interrupt enable. Clearing the local bus cause of the interrupt will clear the interrupt.	Yes	Yes	0
12	Retry Abort Enable. A value of 1 enables the PCI 9060SD to treat 256 Master consecutive retries to a Target as a Target Abort. A value of 0 will enable the PCI 9060SD to attempt Master Retries indefinitely.	Yes	Yes	0
13	A value of 1 indicates the PCI doorbell interrupt is active.	Yes	No	0
14	A value of 1 indicates the PCI abort interrupt is active.	Yes	No	0
15	A value of 1 indicates the local interrupt is active.	Yes	No	0
16	Local interrupt enable. A value of 1 enables Local interrupts.	Yes	Yes	1
17	Local doorbell interrupt enable. A value of 1 enables doorbell interrupts. Used in conjunction with Local interrupt enable. Clearing the local doorbell interrupt bits causing the interrupt will clear the interrupt.	Yes	Yes	0
18	Unused.	Yes	No	0
19	Local DMA channel 1 interrupt enable. A value of 1 enables DMA channel 1 interrupts. Used in conjunction with Local interrupt enable. Clearing the DMA status bits will clear the interrupt.	Yes	Yes	0
20	A value of 1 indicates the Local doorbell interrupt is active.	Yes	No	0
21	Unused.	Yes	No	0
22	A value of 1 indicates the DMA Ch 1 interrupt is active.	Yes	No	0
23	A value of 1 indicates the BIST interrupt is active. The BIST (built in self test) interrupt is generated by writing a 1 to bit 6 of the PCI Configuration BIST register. Clearing bit 6 clears the interrupt. Refer to the BIST register for a description of self test.	Yes	No	0
25:24	Unused.	Yes	No	0
26	A value of 0 indicates a DMA CH1 was the bus master during a Master/Target abort.	Yes	No	0
27	A value of 0 indicates a Target Abort was generated by the PCI 9060SD after 256 consecutive Master retries to a Target.	Yes	No	0
31:28	Reserved.			

4.4.8 EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register (PCI 6Ch) (LOC ECh)

Table 4-41. EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register Description

Field	Description	Read	Write	Value after Reset
3:0	PCI Read Command Code for DMA.	Yes	Yes	1110
7:4	PCI Write Command Code for DMA.	Yes	Yes	0111
11:8	Unused.	—	—	—
15:12	Unused.	—	—	—
16	General Purpose Output. A value of 1 causes USERO output to go high. A value of 0 causes output to go low.	Yes	Yes	1
17	General Purpose Input. A value of 1 indicates the USERI input pin is high. A value of 0 indicates the USERI pin is low.	Yes	No	—
23:18	Unused.	Yes	No	0
24	EEPROM clock for Local or PCI bus reads or writes to EEPROM. Toggling this bit generates an EEPROM clock. Refer to the manufacturer's data sheet for the particular EEPROM being used.	Yes	Yes	0
25	EEPROM chip select. For local or PCI bus reads or writes to EEPROM, setting this bit to a 1 provides the EEPROM chip select.	Yes	Yes	0
26	Write bit to EEPROM. For writes, this output bit is the input to the EEPROM. It is clocked into the EEPROM by the EEPROM clock.	Yes	Yes	0
27	Read EEPROM data bit. For reads, this input bit is the output of the EEPROM. It is clocked out of the EEPROM by the EEPROM clock.	Yes	No	—
28	EEPROM present. A value of 1 indicates an EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When set to 0, writing a 1 causes the PCI 9060SD to reload the local configuration registers from EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. A value of 1 holds the local bus logic in the PCI 9060SD reset and LRESETo# asserted. The contents of the PCI configuration registers and Shared Run Time registers will not be reset. Software Reset can only be cleared from the PCI bus.	Yes	Yes	0
31	Local Init Status. A value of 1 indicates local init done. Responses to PCI accesses will be RETRYs until this bit is set. While Input NB# is asserted low, this bit will be forced to 1.	Yes	Yes	0

4.4.9 PCI Configuration ID Register (PCI 70h) (LOC F0h)

Table 4-42. PCI Configuration ID Register Description

Field	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies the manufacturer of the device. Defaults to the PCI SIG issued vendor ID of PLX (10B5h) if no EEPROM is present and pin NB# (no local bus initialization) is asserted low. *Note: Hardcoded.*	Yes	No	10B5h
31:16	Device ID. Identifies the particular device. Defaults to the PLX part number for PCI interface chip (9060SD) if no EEPROM is present and pin NB# (no local bus initialization) is asserted low. *Note: Hardcoded.*	Yes	No	906D

4.5 LOCAL DMA REGISTERS

Note: DMA Channel 0 is only supported by PCI 9060.

4.5.1 DMA Channel 1 Mode Register (LOC 114h) (PCI 94h)

Table 4-43. DMA Channel 1 Mode Register Description

Field	Description	Read	Write	Value after Reset
1:0	Local Device Bus Width. Programmable for Cx and Jx modes only. A value of 00 indicates a bus width of 8 bits, a value of 01 indicates a bus width of 16 bits, a value of 11 indicates a bus width of 32 bits (or 10 for 32 bit aligned only). The bus width is forced to 16 bits for Sx mode.	Yes	Yes	Sx mode 01 Jx mode 11 Cx mode 11
5:2	Internal Wait States (data to data).	Yes	Yes	0
6	Ready Input Enable. A value of 1 enables Ready input.	Yes	Yes	0
7	Bterm Input Enable. A value of 1 enables Bterm input.	Yes	Yes	0
8	Local Burst Enable. A value of 1 enables Local bursting. A value of 0 disables Local bursting.	Yes	Yes	0
9	Chaining. A value of 1 indicates chaining mode enabled. A value of 0 indicates non-chaining mode enabled.	Yes	Yes	0
10	Done Interrupt Enable. A value of 1 enables interrupt when done. A value of 0 disables interrupt when done.	Yes	Yes	0
11	Local Addressing Mode. A value of 1 indicates local address LA[31:2] to be held constant. A value of 0 indicates local address is incremented.	Yes	Yes	0
12	Demand Mode. A value of 1 causes the DMA controller to operate in demand mode. In demand mode the DMA controller transfers data when its DREQ1# input is asserted. It asserts DACK1# to indicate that the current local bus transfer is in response to the DREQ1# input. The DMA controller transfers Lwords (32 bits) of data. This may result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	Write and Invalidate Mode for DMA transfers: When set to a 1, the PCI 9060SD performs Write and Invalidate cycles to the PCI Bus. The 9060SD supports Write and Invalidate sizes of 8 or 16 Lwords. The size is specified in Table 4-10 for PCI Cache Line Size Register (Offset 0Ch). If a size other than 8 or 16 is specified, the 9060SD performs write transfers rather than Write and Invalidate transfers. Transfers must start and end at the Cache Line Boundaries.	Yes	Yes	0
14	End Of Transfer (EOT) input enable. A value of 1 enables the EOT input pin.	Yes	Yes	0
15	Stop Data Transfer Mode. A value of 1 enables this mode. When this bit is enabled and EOT (bit 14 must be enabled) is received by PCI 9060SD or DREQ1# is de-asserted during demand mode DMA transfer, the PCI 9060SD assumes the current transfer is the last transfer (BLAST# may not be asserted). EOT terminates the transfer. DMA resumes when DREQ1# is reasserted.	Yes	Yes	0
31:16	Reserved.	Yes	No	0

4.5.2 DMA Channel 1 PCI Data Address Register (LOC 118h) (PCI 98h)

Table 4-44. DMA Channel 1 PCI Data Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	PCI Data Address Register. Indicates from where in the PCI memory space the DMA transfers (reads or writes) start.	Yes	Yes	0

4.5.3 DMA Channel 1 Local Data Address Register (LOC 11Ch) (PCI 9Ch)

Table 4-45. DMA Channel 1 Local Data Address Register Description

Field	Description	Read	Write	Value after Reset
31:0	Local Data Address Register. Indicates from where in the local memory space the DMA transfers (reads or writes) start.	Yes	Yes	0

4.5.4 DMA Channel 1 Transfer Size (Bytes) Register (LOC 120h) (PCI A0h)

Table 4-46. DMA Channel 1 Transfer Size (Bytes) Register Description

Field	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to be transferred during DMA operation.	Yes	Yes	0
31:23	Unused.	Yes	No	0

4.5.5 DMA Channel 1 Descriptor Pointer Register (LOC 124h) (PCI A4h)

Table 4-47. DMA Channel 1 Descriptor Pointer Register Description

Field	Description	Read	Write	Value after Reset
0	Reserved.	No	No	0
1	End of Chain. A value of 1 indicates end of chain. A value of 0 indicates not end of chain descriptor.	Yes	Yes	0
2	Interrupt after Terminal Count. A value of 1 causes an interrupt to be generated after the terminal count for this descriptor is reached. A value of 0 disables interrupts from being generated.	Yes	Yes	0
3	Direction of transfer. A value of 1 indicates transfers from local bus to PCI bus. A value of 0 indicates transfers from PCI bus to local bus.	Yes	Yes	0
31:4	Next Descriptor Local Address. Quad word aligned.	Yes	Yes	0

4.5.6 DMA Command/Status Register (LOC 128h) (PCI A8h)

Table 4-48. DMA Command/Status Register Description

Field	Description	Read	Write	Value after Reset
7:0	Unused.	Yes	No	0
8	Channel 1 Enable. A value of 1 enables the channel to transfer data. A value of 0 disables the channel from starting a DMA transfer and if in the process of transferring data suspend transfer (Pause).	Yes	Yes	0
9	Channel 1 Control. A value of 1 causes the channel to start transferring data if the channel is enabled.	No	Yes	0
10	Channel 1 Abort. A value of 1 causes the channel to abort the current transfer. The channel enable bit must cleared. The channel complete bit is set when the abort has completed.	No	Yes	0
11	A value of 1 clears channel 1 interrupts.	No	Yes	0
12	Channel 1 Done. A value of 1 indicates this channel's transfer is complete. A value of 0 indicates the channel transfer is not complete.	Yes	No	1
31:13	Unused.	Yes	No	0

4.5.7 DMA Arbitration Register 0 (LOC 12Ch) (PCI ACh)

Table 4-49. DMA Arbitration Register 0 Description

Field	Description	Read	Write	Value after Reset
7:0	Local Bus Latency Timer. Number of local bus clock cycles before de-asserting HOLD and releasing the local bus.	Yes	Yes	0
15:8	Local Bus Pause Timer. Number of local bus clock cycles before reasserting HOLD after releasing the local bus.	Yes	Yes	0
16	Local Bus Latency Timer Enable. A value of 1 enables the latency timer.	Yes	Yes	0
17	Local Bus Pause Timer Enable. A value of 1 enables the pause timer.	Yes	Yes	0
18	Local Bus BREQ Enable. A value of 1 enables the local bus BREQ input. When the BREQ input is active, the PCI 9060SD de-asserts HOLD and releases the local bus.	Yes	Yes	0
31:19	Unused.	Yes	No	0

4.5.8 DMA Arbitration Register 1 (LOC 130h) (PCI B0h)

Table 4-50. DMA Arbitration Register 1 Description

Field	Description	Read	Write	Value after Reset
15:0	Unused.	—	—	—
19:16	DMA Channel 1 PCI to Local Almost Full (C1PLAF). Number of Full Entries (minus 1) in FIFO before Requesting Local Bus for Writes. (C1PLAF+1) + (C1PLAE+1) should be <= FIFO depth of 16.	Yes	Yes	0
23:20	DMA Channel 1 Local to PCI Almost Empty (C1LPAE). Number of Empty Entries (minus 1) in FIFO before Requesting Local Bus for Reads. (C1PLAF+1) + (C1PLAE+1) should be <= FIFO depth of 16.	Yes	Yes	0
27:24	DMA Channel 1 Local to PCI Almost Full (C1LPAF). Number of Full Entries (minus 1) in FIFO before Requesting PCI Bus for Writes.	Yes	Yes	0
31:28	DMA Channel 1 PCI to Local Almost Empty (C1PLAE). Number of Empty Entries (minus 1) in FIFO before Requesting PCI Bus for Reads.	Yes	Yes	0

5. PIN SUMMARY

Table 5-2 through Table 5-5 describe the PCI 9060SD pins. The pins in the following tables are common to all three local bus modes of operation (Cx, Jx, and Sx modes):

- PCI System Bus Interface Pin Description

- Local Bus Mode and Processor Independent Interface Pin Description

- EEPROM Interface Pin Description

- Power and Ground Pin Description

Table 5-6 through Table 5-8 describe the local bus mode of the PCI 9060SD:

- Cx Bus Mode Interface Pin Description (i960® Cx and Hx processors)

- Jx Bus Mode Interface Pin Description (i960® Jx and Kx processors)

- Sx Bus Mode Interface Pin Description (i960® Sx processor)

Unspecified pins are no connects.

Table 5-1 lists the abbreviations used in this section to represent the various pin types.

Table 5-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output pin
I	Input pin only
O	Output pin only
TS	Tri-state pin
OC	Open collector pin
TP	Totem pole pin
STS	Sustained tri-state pin, driven high for one CLK before float
DTS	Driven Tri-state Pin, driven high for 1/2 CLK before float

All local bus inputs (Pin Type I) are internally connected to Vcc through a 10k ohm pull-up resistor.

Exceptions:

1. The TEST and BREQ pins have a 10k ohm pull-down resistor.

2. The EOT1# pin does not have any pull-up or pull-down resistor.

All local tri-state I/O pins should have pull-ups.

Design Notes: PULL up/down (use 3k - 10kΩ).

For PCI Pins, DO NOT pull up/down any pins unless you are using the PCI 9060SD for an embedded design.

Refer to *PCI Local Bus Specification*, Revision 2.1, page 123.

Table 5-2. Power and Ground Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
TEST	Test	1	I	49	Test Pin. Pull high for test, low for normal operation. When TEST is pulled high, all outputs except USERO (pin 27) are placed in tri-state. USERO provides a NAND-TREE output when TEST is pulled high.
VDD	Power	12	I	1, 38, 53, 60, 68, 83, 105, 124, 144, 157, 167,184	Five volt power supply pins. Liberal .01 µF to .1 µF decoupling capacitors should be placed near the PCI 9060SD.
VSS	Ground	20	I	22, 37, 45, 52, 59, 67, 75, 82, 90, 98, 104, 114, 123, 134, 143, 156, 166, 183, 193, 208	Ground pins.

Table 5-3. EEPROM Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
CLKSEL	Clock Select	1	I	170	When set to 0 EE1MC will be used to clock the EEPROM. When set to 1 an internally generated clock will be used to clock the EEPROM. The clock is generated from the PCI Clock.
EE1MC	1 MHz Clock	1	I	175	Optional EEPROM clock source.
EECS	EEPROM Chip Select	1	O TP 6 mA	176	EEPROM chip select.
EEDI	EEPROM Data In	1	O TP 6 mA	172	Write data to EEPROM.
EEDO	EEPROM Data Out	1	I	171	Read data from EEPROM.
EESK	Serial Data Clock	1	O TP 6 mA	173	EEPROM Clock
SHORT#	Load Short	1	I	174	When active low only five 32-bit registers are loaded from the EEPROM. When active high all local configuration registers are also loaded from EEPROM.

Table 5-4. PCI System Bus Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS 6 mA	32-36, 39-44, 46-47, 76-81, 84-89, 91-97	These are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The PCI 9060SD supports both read and write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I/O TS 6 mA	70-73	These are multiplexed on the same PCI pins. During the address phase of a transaction C/BE[3:0]# define the bus command. During the data phase C/BE[3:0]# are used as Byte Enables. Refer to PCI spec for further detail if needed.
CLK	Clock	1	I	54	This provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33 MHz.
DEVSEL#	Device Select	1	I/O STS 6 mA	64	When a device has decoded its address as the target of the current access, the device asserts DEVSEL#. As an input, DEVSEL# indicates whether any device on the bus has been selected.
FRAME#	Cycle Frame	1	I/O STS 6 mA	57	This is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is de-asserted, the transaction is in the final data phase.
GNT#	Grant	1	I	51	This indicates to the agent that access to the bus has been granted. Every master has its own REQ# and GNT#.
IDSEL	Initialization Device Select	1	I	63	This is used as a chip select during configuration read and write transactions.
INTA#	Interrupt A	1	O OC 6 mA	55	This is used to request an interrupt.
IRDY#	Initiator Ready	1	I/O STS 6 mA	61	This indicates the ability of the initiating agent (bus master) to complete the current data phase of the transaction.
LOCK#	Lock	1	I	69	LOCK# indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS 6 mA	74	This is even parity across AD[31:0] and C/BE[3:0]#. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase.
PERR#	Parity Error	1	I/O STS 6 mA	65	This is only the reporting of data parity errors during all PCI transactions except a Special Cycle.
REQ#	Request	1	O 6 mA	50	This indicates to the arbiter that this agent wants use of the bus. Every master has its own GNT# and REQ#.
RST#	Reset	1	I	56	This is used to bring PCI-specific registers, sequencers, and signals to a consistent state.

Table 5-4. PCI System Bus Interface Pin Description (continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
SERR#	Systems Error	1	O OC 6 mA	66	This is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
STOP#	Stop	1	I/O STS 6 mA	62	This indicates the current target is requesting the master to stop the current transaction.
TRDY#	Target Ready	1	I/O STS 6 mA	58	This indicates the ability of the target agent (selected device) to complete the current data phase of the transaction.

Table 5-5. Local Bus Mode and Processor Independent Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADMODE	Address Decode Mode	1	I	20	Determines how S[2:0] are used to access the PCI 9060SD internal registers
BIGEND#	Big Endian Select	1	I	48	BIGEND# can be asserted during the local bus address phase of a Direct Master transfer or a configuration register access to specify that Big Endian byte ordering should be used. Big Endian byte order for Direct Master transfers or configuration register accesses is also programmable through configuration registers.
BPCLKO	Buffered PCI Clock Output	1	O TP 6 mA	168	BPCLKO provides a buffered PCI clock output.
BREQ	Bus Request	1	I	169	BREQ is asserted to indicate that a local bus master requires the bus. If enabled through the PCI 9060SD configuration registers, the PCI 9060SD will release the bus if this signal is asserted.
DREQ1#	DMA Request Input	1	I	24	When a channel is programmed through the configuration registers to operate in demand mode, its REQ input serves as a DMA request
DACK1#	DMA Request Output	1	O TP 6 mA	25	When a channel is programmed through the configuration registers to operate in demand mode, its DACK output indicates a DMA transfer is being executed.
DP[3:0]	Data Parity	4	I/O TS 6 mA	12-15	Parity is even for each of up to 4 byte lanes on the local bus. Parity is checked for writes to the PCI 9060SD or reads by the PCI 9060SD. Parity is generated for reads from the PCI 9060SD or writes by the PCI 9060SD.
LDSHOLD	Direct Slave HOLD Request	1	O TP 6 mA	165	Asserted coincident with LHOLD to indicate that the PCI 9060SD is requesting use of the Local Bus in order to perform a Direct Slave transfer.
LINTi#	Local Interrupt In	1	I	151	When asserted low causes a PCI interrupt.
LINTo#	Local Interrupt Out	1	O TP 6 mA	152	The interrupt output is a synchronous level output. The output will remain asserted as long as an interrupt condition exists. If an edge level interrupt is required, disabling and then enabling local interrupts though the interrupt/control status register will create an edge if an interrupt condition still exists or a new interrupt condition occurs.
LLOCKo#	Bus Lock	1	O TP 6 mA	7	This output indicates an atomic operation for a (Direct Slave) PCI to local bus access may require multiple transactions to complete.
LRESETi#	Local Reset In	1	I	150	This pin resets the local bus portion of the PCI 9060SD chip and causes the local reset output to be asserted.

Table 5-5. Local Bus Mode and Processor Independent Interface Pin Description (continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LSERR#	System Error	1	O TP 6 mA	23	The LSERR# interrupt output is a synchronous level output. LSERR# interrupt output is asserted when the PCI bus Target Abort or Master Abort status bit is set in the PCI Status Configuration Register. If an edge level interrupt is required, disabling and then enabling LSERR# interrupts though the interrupt/control status will create an edge if an interrupt condition still exists or a new interrupt condition occurs.
MODE[1:0]	Bus Mode	2	I	9-10	Selects the bus operation mode of the PCI 9060SD: Bit 1 Bit 0 Bus Mode 　0　　　0　　　　Cx 　0　　　1　　　　Jx 　1　　　0　　　　Sx 　1　　　1　　　Reserved
NB#	No Local Bus Initialization	1	I	26	Externally sets local init done. Init done is also programmable through configuration registers.
PCHK#	Data Parity Check	1	O TP 6 mA	16	Parity is checked for writes to the PCI 9060SD or reads by the PCI 9060SD. Parity is checked for each byte lane with its byte enable asserted. PCHK# is asserted in the clock cycle following the data being checked if a parity error is detected.
S[2:0]	Address Select	3	I	17-19	If ADMODE is high, internal PCI 9060SD registers are selected when LA[31:29] match S[2:0]. If ADMODE is low, the internal PCI 9060SD registers are selected when S0 is asserted low.
USERI	User Input	1	I	31	This is a general purpose input that can be read from the PCI 9060SD configuration registers.
USERO	User Output	1	O TP 24 mA	27	This is a general purpose output controlled from the PCI 9060SD configuration registers.
WAITI#	Wait Input	1	I	6	WAITI# can be asserted to cause the PCI 9060SD to insert wait states for local direct master accesses to the PCI bus. WAITI# can be thought of as a ready input for direct master accesses.
WAITO#	Wait Out	1	O T 6 mA	149	This output indicates the PCI 9060SD programmable wait state generator status. WAITO# is asserted when wait states are being caused by the internal wait state generator. It can be thought of as an output providing ready out status.

Table 5-6. Cx Bus Mode Interface Pin Description

Cx Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	I/O TS 24 mA	154	Address strobe indicates valid address and the start of a new bus access. ADS# is asserted for the first clock of a bus access.
BLAST#	Burst Last	1	I/O TS 6 mA	155	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
BTERM#	Burst Terminate	1	I	146	The i960® Cx processor bursts up to 4 Lwords. If BTERM# is disabled through the PCI 9060SD configuration registers, the PCI 9060SD will also burst up to 4 Lwords. If enabled, the PCI 9060SD will continue to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the PCI 9060SD programmable wait state generator.
DEN#	Data Enable	1	O TS 24 mA	145	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus.
DT/R#	Data Transmit/Receive	1	O TS 24 mA	138	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus. When asserted the signal indicates the PCI 9060SD receives data.
LW/R#	Write/Read	1	I/O TS 24 mA	137	LW/R# is asserted low for reads and is high for writes.
LA[31:2]	Address Bus	30	I/O TS 6 mA	136-135, 133-125, 122-115, 113-106, 103-101	Address bus carries the upper 30 bits of the physical address bus. During bursts, LA[3:2] increment to indicate successive data cycles.

Table 5-6. Cx Bus Mode Interface Pin Description (continued)

Cx Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LD[31:0]	Data Bus	32	I/O TS 6 mA	177-182, 185-192, 194-207, 2-5	Data bus carries 32, 16, or 8 bit data quantities depending on bus width configuration.
LBE[3:0]#	Byte Enables	4	I/O TS 24 mA	139-142	The byte enables are encoded based on configured bus width as follows: **32-Bit Bus** The four byte enables indicate which of the four bytes are active during a data cycle. BE3# Byte Enable 3 - LD[31:24] BE2# Byte Enable 2 - LD[23:6] BE1# Byte Enable 1 - LD[15:8] BE0# Byte Enable 0 - LD[7:0] **16-Bit Bus** BE3#, BE1#, and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively. BE3# Byte High Enable (BHE#) - LD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#) - LD[7:0] **8-Bit Bus** BE1# and BE0# are encoded to provide LA1 and LA0, respectively. BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)
LCLK	Local Processor Clock	1	I	160	Local clock or i960® Cx processor PCLK1 or PCLK2 output
LHOLD	Hold Request	1	O TP 6 mA	158	The PCI 9060SD asserts LHOLD to request use of the local bus. The i960® Cx processor or local bus arbiter asserts LHOLDA when control has been granted.
LHOLDA	Hold Acknowledge	1	I	159	The PCI 9060SD asserts LHOLD to request use of the local bus. The i960® Cx processor or local bus arbiter asserts LHOLDA when control has been granted. The bus should not be granted to the PCI 9060SD unless requested by LHOLD.
LRESETo#	Local Reset Out	1	O TP 6 mA	11	This pin is the Local bus reset output. It is asserted when the PCI 9060SD chip is reset. It is used to drive the RESET# input of the local processor.
READYi#	Ready In	1	I	147	When the PCI 9060SD is a bus master, READYi# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYi# is used in conjunction with the PCI 9060SD programmable wait state generator.
READYo#	Ready Out	1	O DTS 6 mA	148	When a local bus access is made to the PCI 9060SD, READYo# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYo# can be connected to READYi#.
EOT1#	End Of Transfer for DMA CH1	1	I	164	EOT1# causes the termination of a current DMA CH1 transfer.

Table 5-7. Jx Mode Bus Interface Pin Description (Also used for Kx processor interface)

Jx Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ALE	Address Latch Enable	1	O TS 6 mA	161	ALE is asserted during the address phase and de-asserted before the data phase.
ADS#	Address Strobe	1	I/O TS 24 mA	154	Address strobe indicates valid address and the start of a new bus access. ADS# is asserted for the first clock of a bus access.
BLAST#	Burst Last	1	I/O TS 6 mA	155	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
BTERM#	Burst Terminate	1	I	146	The i960® Jx processor bursts up to 4 Lwords. If BTERM# is disabled through the PCI 9060SD configuration registers, the PCI 9060SD will also burst up to 4 Lwords. If enabled, the PCI 9060SD will continue to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the PCI 9060SD programmable wait state generator.
DEN#	Data Enable	1	I/O TS 24 mA	145	As an input, DEN# must only be asserted during data phases. In i960® Kx systems, DEN# is used internally to block i960® Kx processor assertions of ADS# during data phases of a burst. For non i960® Kx processor systems or systems in which ADS# is not asserted during the data phase, DEN# can be pulled high. As an output, DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus.
DT/R#	Data Transmit/Receive	1	O TS 24 mA	138	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus. When asserted the signal indicates the PCI 9060SD receives data.
LW/R#	Write/Read	1	I/O TS 24 mA	137	LW/R# is asserted low for reads and is high for writes.
LABS[3:2]	Address Bus Burst	2	I/O TS 6 mA	162-163	Carries the word address of the 32 bit memory address. These bits are incremented during a burst access.

Table 5-7. Jx Mode Bus Interface Pin Description (Also used for Kx processor interface) (continued)

Jx Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LAD[31:0]	Address/Data Bus	32	I/O TS 6 mA	136-135, 133-125, 122-115, 113-106, 103-99	During the address phase the bus carries the upper 30 bits of the physical address bus. During the data phase, the bus carries 32 bits of data.
LBE[3:0]#	Byte Enables	4	I/O TS 24 mA	139-142	The byte enables are encoded based on configured bus width as follows: **32-Bit Bus** The four byte enables indicate which of the four bytes are active during a data cycle. BE3# Byte Enable 3 - LAD[31:24] BE2# Byte Enable 2 - LAD[23:16] BE1# Byte Enable 1 - LAD[15:8] BE0# Byte Enable 0 - LAD[7:0] **16-Bit Bus** BE3#, BE1#, and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively. BE3# Byte High Enable (BHE#) - LAD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#) - LAD[7:0] **8-Bit Bus** BE1# and BE0# are encoded to provide LA1 and LA0, respectively. BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)
LCLK	System Clock	1	I	160	Local clock or i960® Jx processor clock.
LHOLD	Hold Request	1	O TP 6 mA	158	The PCI 9060SD asserts LHOLD to request use of the local bus. The i960® Jx processor or local bus arbiter asserts LHOLDA when control has been granted.
LHOLDA	Hold Acknowledge	1	I	159	The PCI 9060SD asserts LHOLD to request use of the local bus. The i960® Jx processor or local bus arbiter asserts LHOLDA when control has been granted. The bus should not be granted to the PCI 9060SD unless requested by LHOLD.
LRESETo#	Local Reset Out	1	O TP 6 mA	11	This pin is the Local bus reset output. It is asserted when the PCI 9060SD chip is reset.
READYi#	Ready In	1	I	147	When the PCI 9060SD is a bus master, READYi# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYi# is used in conjunction with the PCI 9060SD programmable wait state generator.
READYo#	Ready Out	1	O DTS 6 mA	148	When a local bus access is made to the PCI 9060SD, READYo# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYo# can be connected to READYi#.
EOT1#	End Of Transfer for DMA CH1	1	I	5	EOT1# causes the termination of a current DMA CH1 transfer.

Table 5-8. Sx Mode Interface Pin Description

Sx Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ALE	Address Latch Enable	1	O TS 6 mA	161	ALE is asserted during the address phase and de-asserted before the data phase.
AS#	Address Strobe	1	I/O TS 24 mA	154	Address strobe indicates valid address and the start of a new bus access. AS# is asserted for the first clock of a bus access.
BLAST#	Burst Last	1	I/O TS 6 mA	155	BLAST# is a signal driven by the current local bus master to indicate the last transfer in a bus access.
BTERM#	Burst Terminate	1	I	146	The i960® Sx processor does not use a BTERM# input. It bursts up to 8 words. If BTERM# is disabled through the PCI 9060SD configuration registers, the PCI 9060SD will also burst up to 8 words. If enabled, the PCI 9060SD will continue to burst until a BTERM# input is asserted. BTERM# breaks up a burst cycle and causes another address cycle to occur. BTERM# is used in conjunction with the PCI 9060SD programmable wait state generator.
DEN#	Data Enable	1	O TS 24 mA	145	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus.
DT/R#	Data Transmit/Receive	1	O TS 24 mA	138	DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to the local bus. When asserted the signal indicates the PCI 9060SD receives data.
LA[31:16]	Address Bus	16	I/O TS 6 mA	136-135, 133-125, 122-118	Carries the upper 32 bits of the address.
LABS[3:1]	Address Bus Burst	3	I/O TS 6 mA	162-164	Carries the word address of the 32 bit memory address. These bits are incremented during a burst access.
LAD[15:1],D0	Address/Data Bus	16	I/O TS 6 mA	117-115, 113-106, 103-99	During the address phase the bus carries the lower physical address bits. During the data phase, the bus carries 16 bits of data.
LBE[1:0]#	Byte Enables	2	I/O TS 24 mA	141-142	Byte enables indicate which of the two bytes are active during a data cycle.
LCLK	System Clock	1	I	160	CLK2 input of the i960® Sx processor. The RESET# input of the i960® Sx processor must be connected to the PCI 9060SD LRESETo# output. This enables the PCI 9060SD to determine the phase of the 2x clock processor.

Table 5-8. Sx Mode Interface Pin Description (continued)

Sx Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LHOLD	Hold Request	1	O TP 6 mA	158	The PCI 9060SD asserts LHOLD to request use of the local bus. The i960® Sx processor or local bus arbiter asserts LHOLDA when control has been granted.
LHOLDA	Hold Acknowledge	1	I	159	The PCI 9060SD asserts LHOLD to request use of the local bus. The i960® Sx processor or local bus arbiter asserts LHOLDA when control has been granted. The bus should not be granted to the PCI 9060SD unless requested by LHOLD.
LRESETo#	Local Reset Out	1	O TP 6 mA	11	This pin is the Local bus reset output. It is asserted when the PCI 9060SD chip is reset. Note: this output must be used to drive the Reset Input of the i960® Sx processor. This enables the PCI 9060SD to determine the phase of the 2x clock processor.
LW/R#	Write/Read	1	I/O TS 24 mA	137	LW/R# is asserted low for reads and is high for writes.
READYi#	Ready In	1	I	147	When the PCI 9060SD is a bus master, READYi# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYi# is used in conjunction with the PCI 9060SD programmable wait state generator.
READYo#	Ready Out	1	O DTS 6 mA	148	When a local bus access is made to the PCI 9060SD, READYo# is used to indicate that read data on the bus is valid or that a write data transfer has completed. READYo# can be connected to READYi#.
EOT1#	End Of Transfer for DMA CH1	1	I	5	EOT1# causes the termination of a current DMA CH1 transfer.

6. ELECTRICAL AND TIMING SPECIFICATIONS

Table 6-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-65 °C to + 150 °C
Ambient Temperature with Power Applied	-55 °C to + 125 °C
Supply Voltage to Ground	-0.5 V to +7.0 V
Input Voltage (VIN)	VSS -0.5 V VDD +0.5 V
Output Voltage (VOUT)	VSS -0.5 V VDD +0.5 V

Table 6-2. Operating Ranges

Ambient Temperature	Junction Temperature	Supply Voltage (VDD)	Input Voltage (VIN)
0 °C to +70 °C	115 °C Maximum	5 V ±5%	Min = VSS Max = VDD

Table 6-3. Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0 V f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0 V f = 1 MHz	Output	10	pF

Table 6-4. Electrical Characteristics Tested over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	VDD = Min,	IOH = -4.0 mA	2.4	—	V
VOL	Output Low Voltage	VIN = VIH or VIL	IOL per Tables	—	0.4	V
VIH	Input High Level			2.0	—	V
VIL	Input Low Level			—	0.8	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD VDD = Max		-10	+10	µA
IOZ	Tri-state Output Leakage Current	VDD = Max VSS ≤ VIN ≤ VDD		-10	+10	µA
ICC	Power Supply Current	VDD = 5.25 V, PCLK = LCLK = 33 MHz		—	130	mA
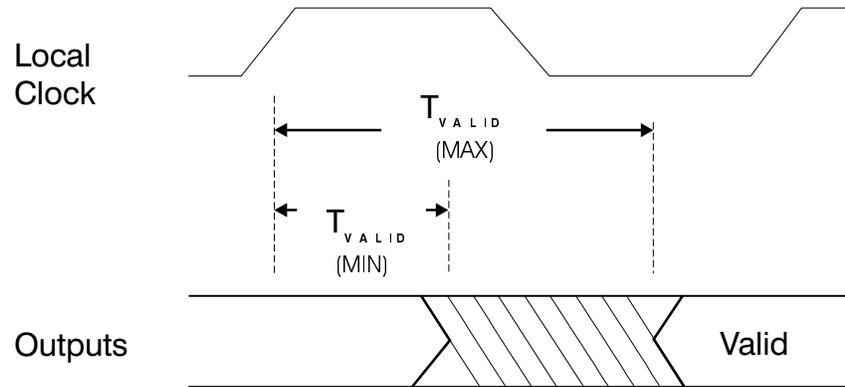
Figure 6-1. PCI 9060SD Local Output Delay

Table 6-5. AC Electrical Characteristics (Local Outputs) Measured over Operating Range

Signals (Synchronous Outputs) CL = 50 pF, VCC = 5.0 ± 5%	$T_{VALID (MIN)}$ NSEC (HOLD)	$T_{VALID (MAX)}$ NSEC (WORST CASE)
LHOLD	5	17
LDSHOLD	5	16
ADS#	6	13
BLAST#	8	16
LBE[3:0]#	8	16
LW/R#	6	17
LD[31:0]	9	20
LA[31:0]	8	20
DT/R#	6	17
DEN#	5	13
READY#	5	14
DP[3:0]	12	20
LRESETo#	5	17
LAD[31:0] (Jx and Sx modes)	9	20
LABS[3:1] (Jx and Sx modes)	8	20
LINT#	5	16
LSERR#	9	16
PCHK#	6	20
USERO	5	21
WAITO#	6	14
DACK1#	5	14.3
LALE (Jx and Sx modes) (address setup and hold relative to LALE negative edge)	5	—
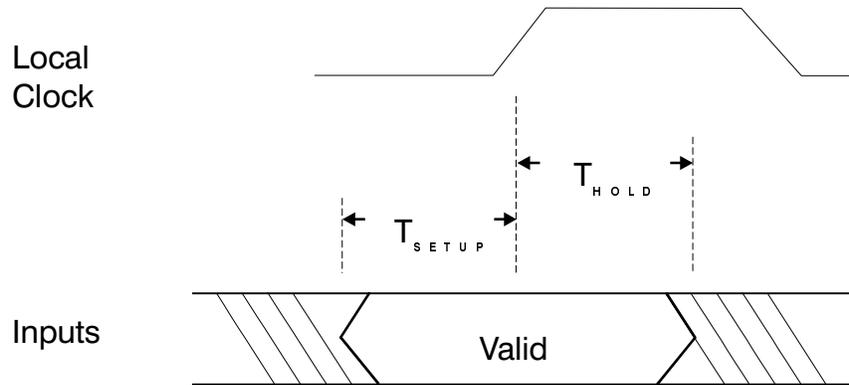
Figure 6-2. PCI 9060SD Local Input Setup and Hold Waveform

Table 6-6. AC Electrical Characteristics (Local Inputs) Measured over Operating Range

Signals (Synchronous Inputs) CL = 50 pF, VCC = 5.0 ± 5%	T_{SETUP} (NSEC) [JM3]	T_{HOLD} (NSEC) (WORST CASE)
LHOLDA	5	1
ADS#	9	1
BLAST#	6	1
LD[31:0]	7	1
LA[31:0]	2	—
DP[3:0]	4	1
BTERM#	5	1
READYi#	9	1

Table 6-7. Clock Frequencies

Frequency	Min	Max
Local Clock Input Frequency	0	40 MHz
PCI Clock Input Frequency	0	33 MHz

7. PACKAGE SPECIFICATIONS

7.1 PACKAGE MECHANICAL DIMENSIONS

For 208 PQFP, θJC = 5 °C/Watt
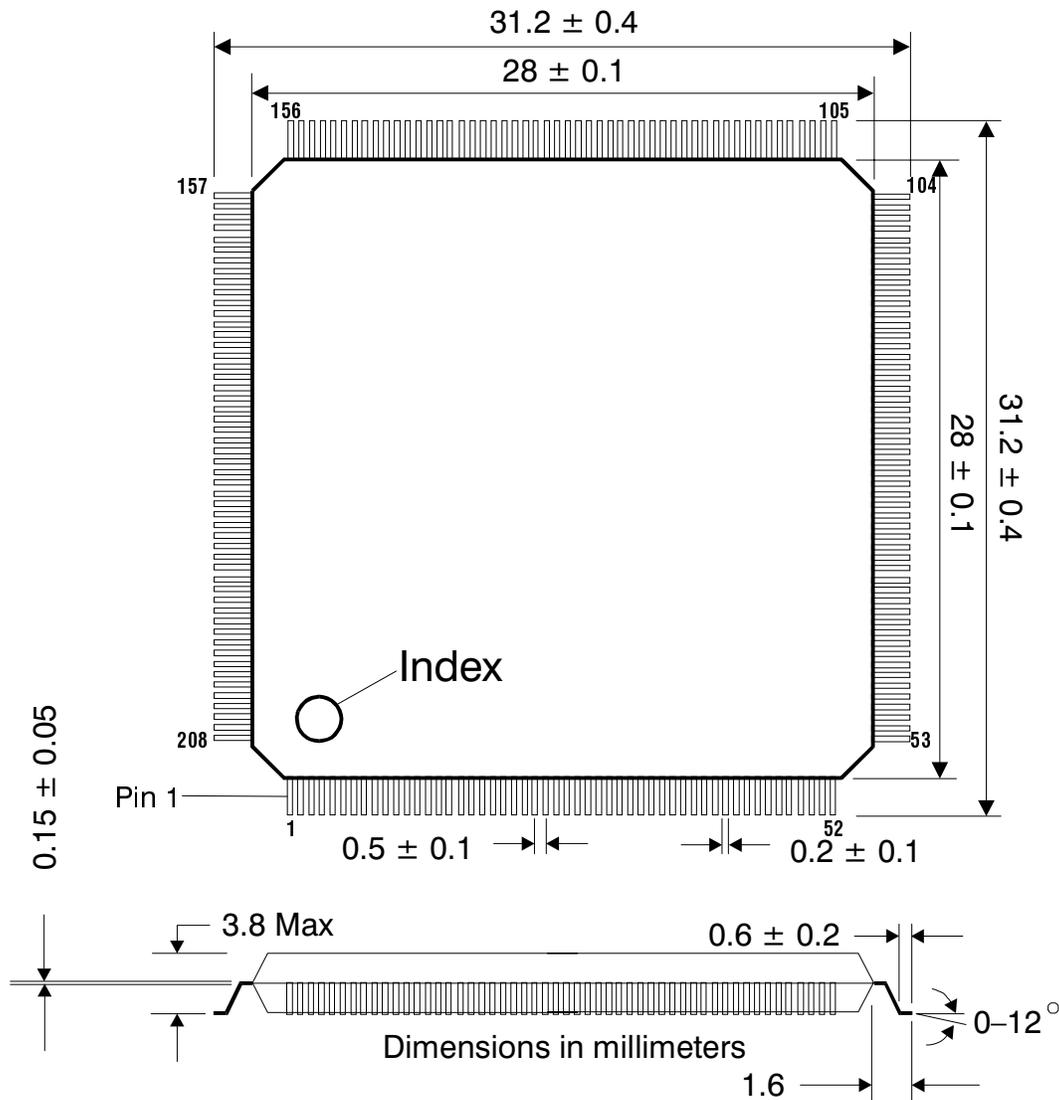
Figure 7-1. Package Mechanical Dimensions

7.2 TYPICAL PCI BUS MASTER ADAPTER
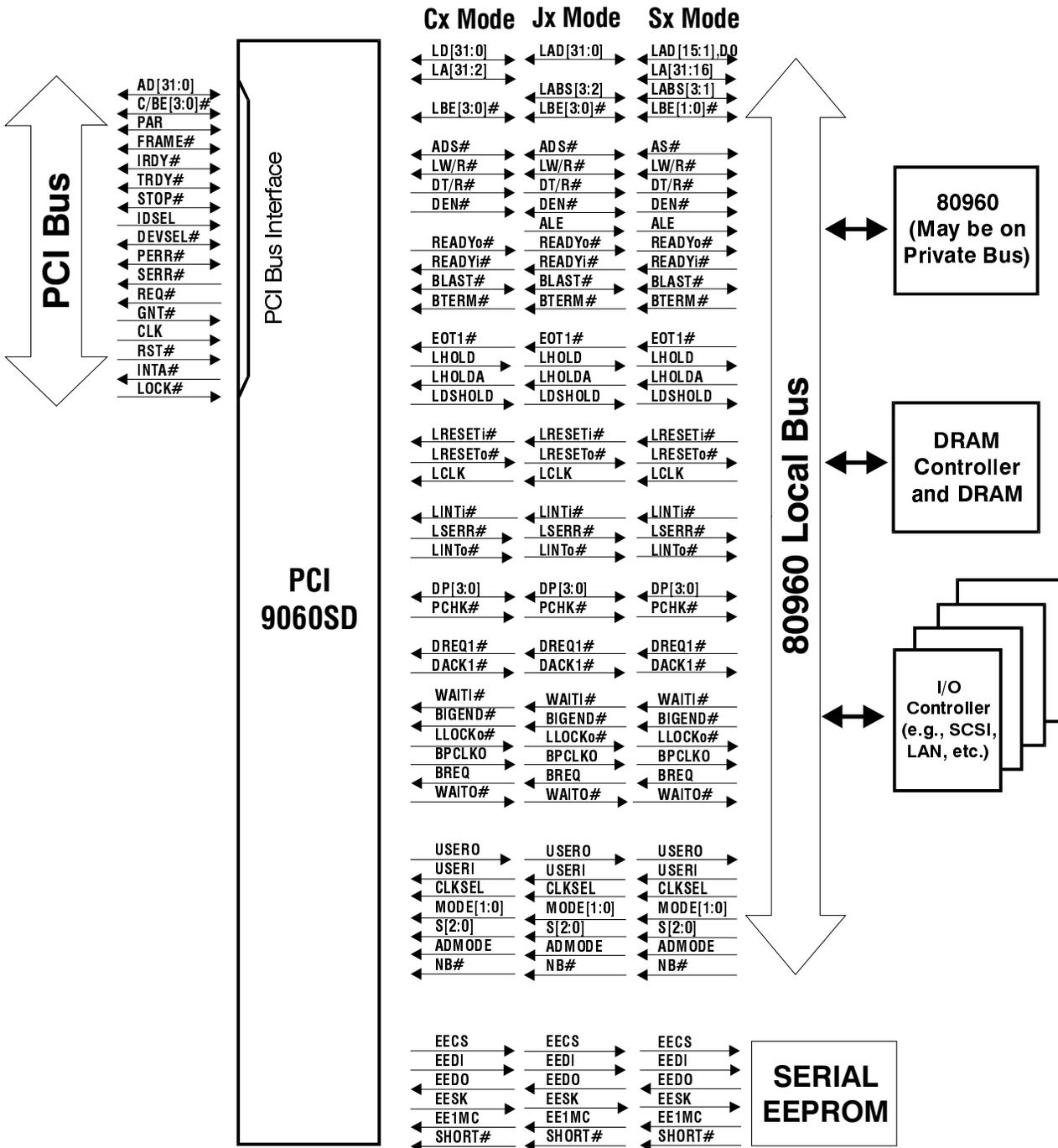
Figure 7-2. Typical PCI Bus Master Adapter

7.3 PCI 9060SD PIN OUT

Sx

Jx

Cx

PCI 9060SD

Figure 7-3. PCI 9060SD Pin Out

8. TIMING DIAGRAMS

The PCI 9060SD operates in three modes, selected through mode pins, corresponding to three processor types—Cx, Jx, and Sx. Timing Diagrams are provided for the three operating modes. For some functions, a timing diagram may only be provided for one mode of operation. Even though a different mode is used, that timing diagram can be used to determine functionality.

8.1 LIST OF TIMING DIAGRAMS

Timing Diagram 8-1. Initialization from Serial EEPROM

0ns		250ns		500ns

LCLK

LHOLD   WILL NOT BE REASSERTED UNITL LHOLDA GOES LOW

LDSHOLD   HIGH IF DIRECT SLAVE REQUEST

LHOLDA |--- CAN GO HIGH
                MUST REMAIN HIGH UNTIL LHOLD
                GOES LOW

LOCAL BUS   PCI 9060SD DRIVES

PCI 9060SD always gives up bus between different local bus accesses:

different direct slave access, different DMA access, between direct slave/DMA accesses.

Timing Diagram 8-2. PCI 9060SD Local Bus Arbitration

100ns	200ns	300ns	400ns	500n

PCI CLK

FRAME#

                                                                BIT [15]=1 INDICATES LINTi# IS ACTIVE

AD[31:0]   ADDR   DATA

C/BE[3:0]#   CMD   BE

IRDY#

DEVSEL#

TRDY#

INTA#   RESPONSE ON THE PCI SIDE

                    [3,15]

LCLK

LINTi#

Timing Diagram 8-3. Local LINTi# Input Asserting PCI Output INTA#

Timing Diagram 8-4. (Cx and Jx Mode) PCI RST# Asserting Local Output LRESETo#

Note: First READYo# will be delayed for access to shared registers, S0 = CS#.

Timing Diagram 8-5. (Cx Mode) Local Bus Write to PCI 9060SD Configuration Register

Note: First READYo# will be delayed for access to shared registers, S0 = CS#.

Timing Diagram 8-6. (Cx Mode) Local Bus Read from PCI 9060SD Configuration Register

Unused read data is flushed.

(No wait states, 32-bit bus, burst enabled, Bterm disabled, Local Bursts of 4 Lwords at a time)
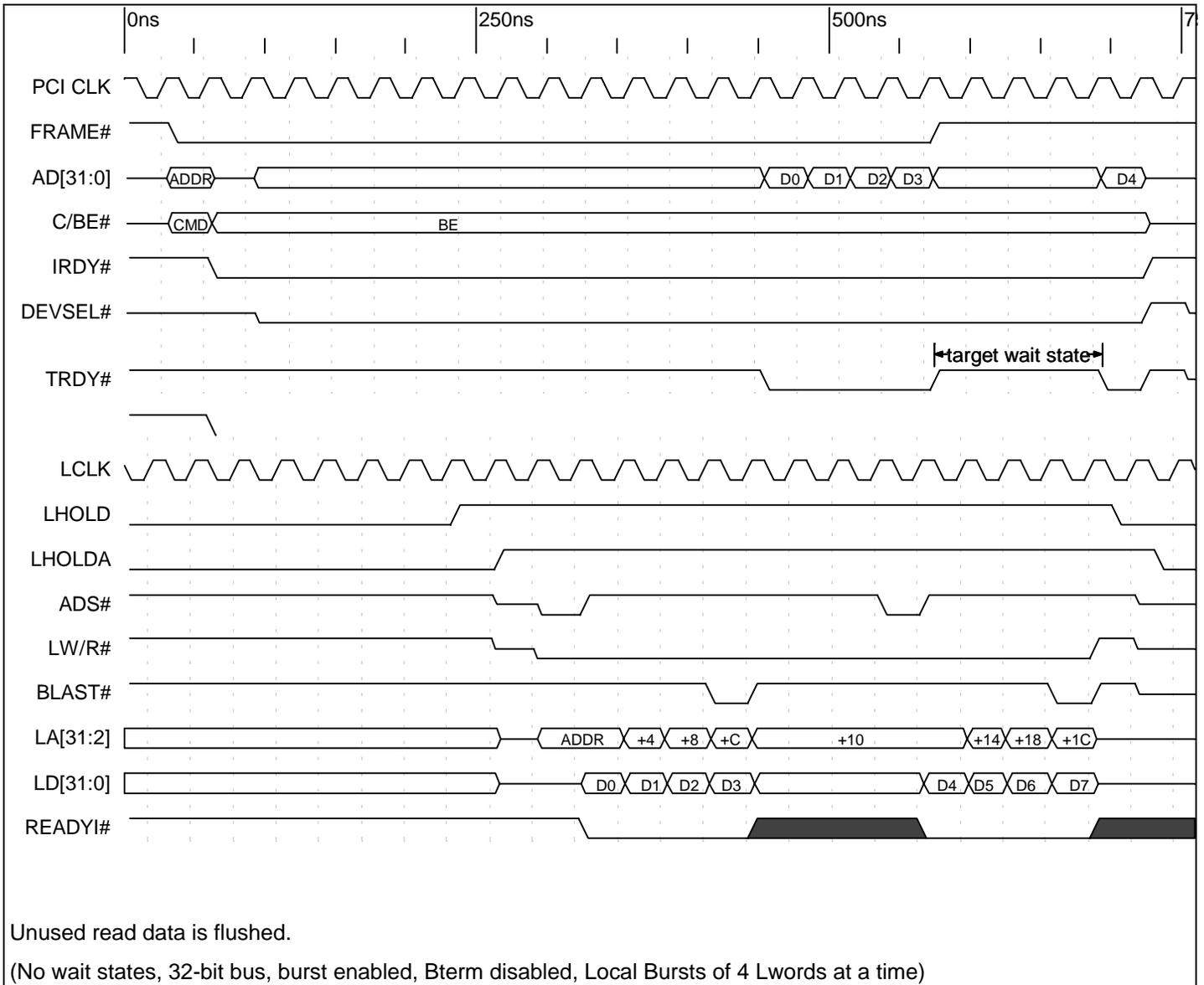
Timing Diagram 8-7. (Cx Mode) Direct Slave PCI to Local Burst Read of 5

Note: If Bterm is disabled, a new ADS (address) cycle starts every quad word boundary.

(No wait states, 32-bit bus, burst enabled, Bterm enabled)
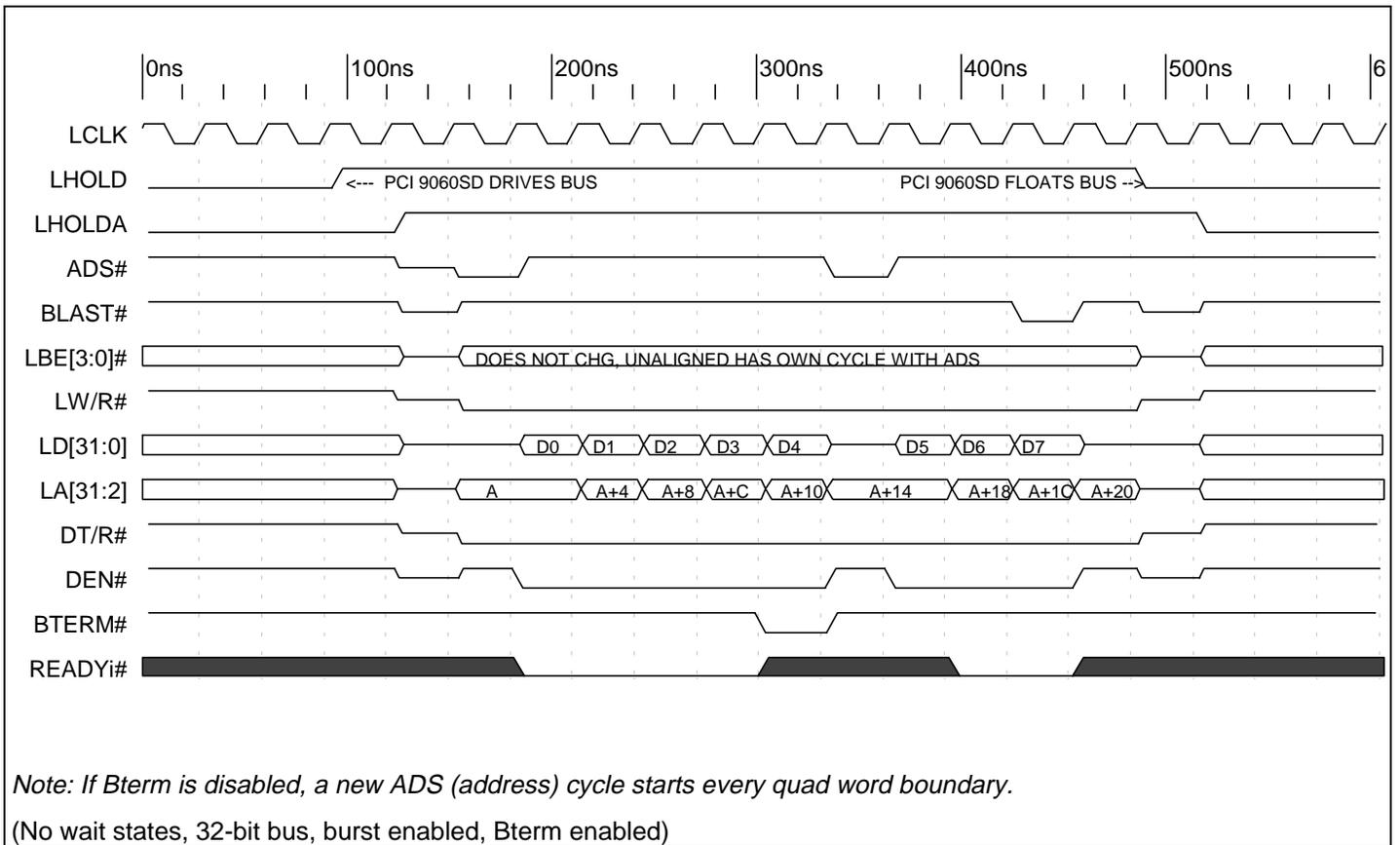
Timing Diagram 8-8. (Cx Mode) PCI 9060SD DMA or Direct Slave Burst Read, Bterm Enabled

	0ns	100ns	200ns	300ns	400ns	500

LCLK

LHOLD <--- PCI 9060SD DRIVES BUS   PCI 9060SD FLOATS BUS -->

LDSHOLD LDSHOLD IS LOW FOR DMA,   HIGH FOR DIRECT SLAVE ACCESS

LHOLDA

ADS#

BLAST#

LBE[3:0]# 0000

LW/R#

LD[31:0] D0 D1 D2 D3

LA[31:2] A A+4 A+8 A+C A+10

DT/R#

DEN#

BTERM#

READYi#

(32 Bit Local Bus, burst enabled, Bterm disabled)
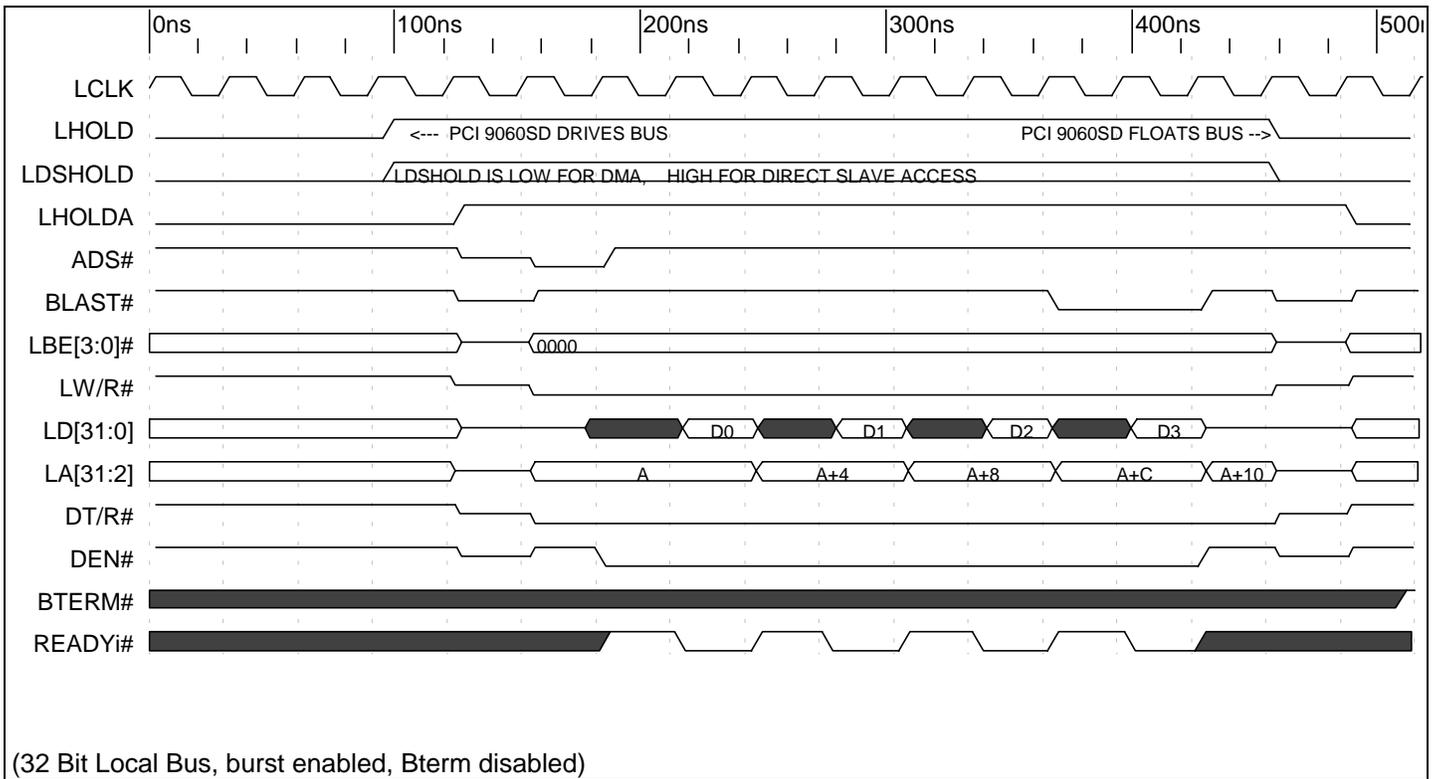
Timing Diagram 8-9. (Cx Mode) Direct Slave or DMA Burst Read from Local Bus (1 External Wait State)

If ready input is enabled in bus region register, additional wait states can be asserted externally.

(32 Bit Local Bus, burst enabled, Bterm Disabled)
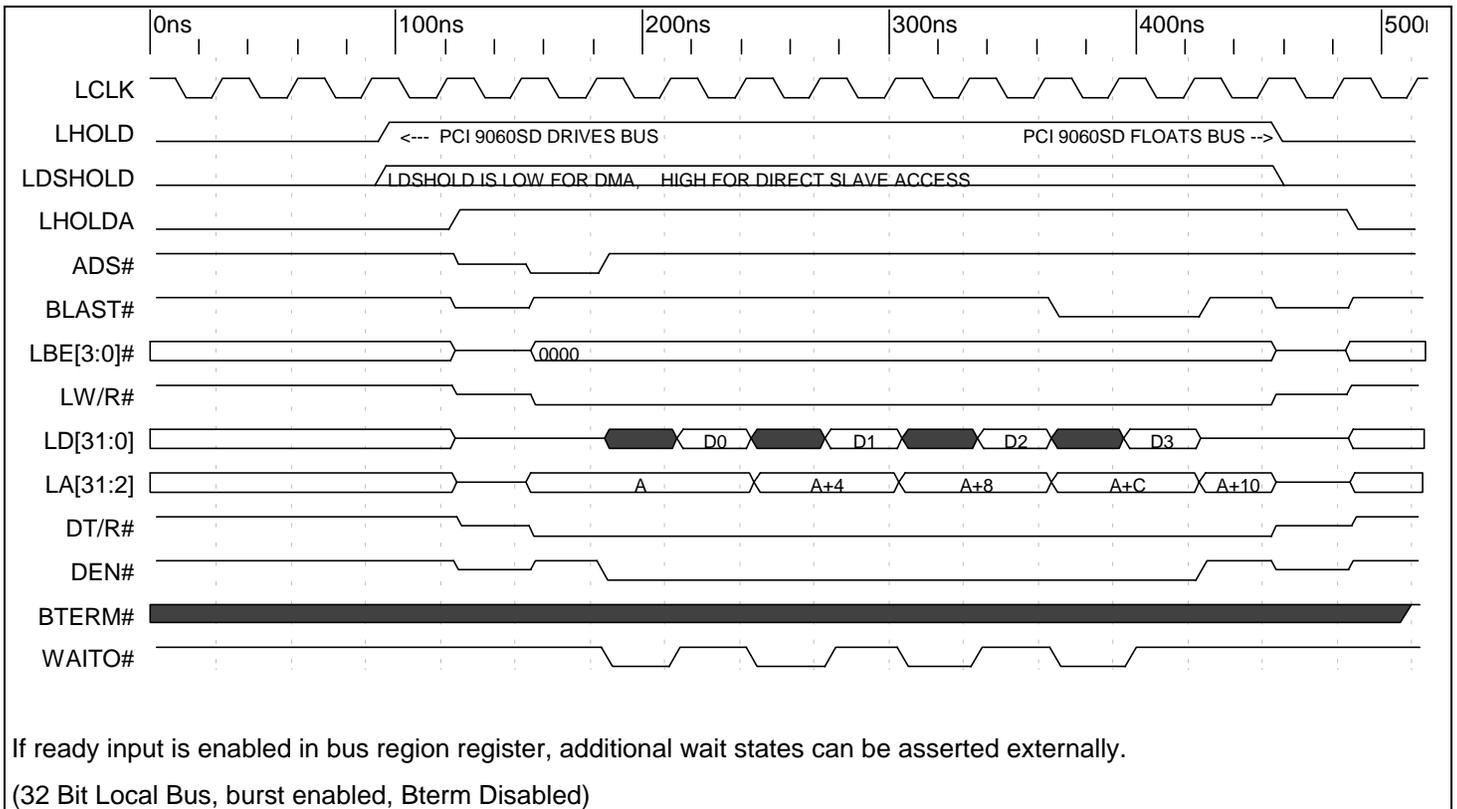
Timing Diagram 8-10. (Cx Mode) Burst Read from Local Bus (1 Internal Wait State Programmed)

(32 Bit Local Bus, Without Burst)
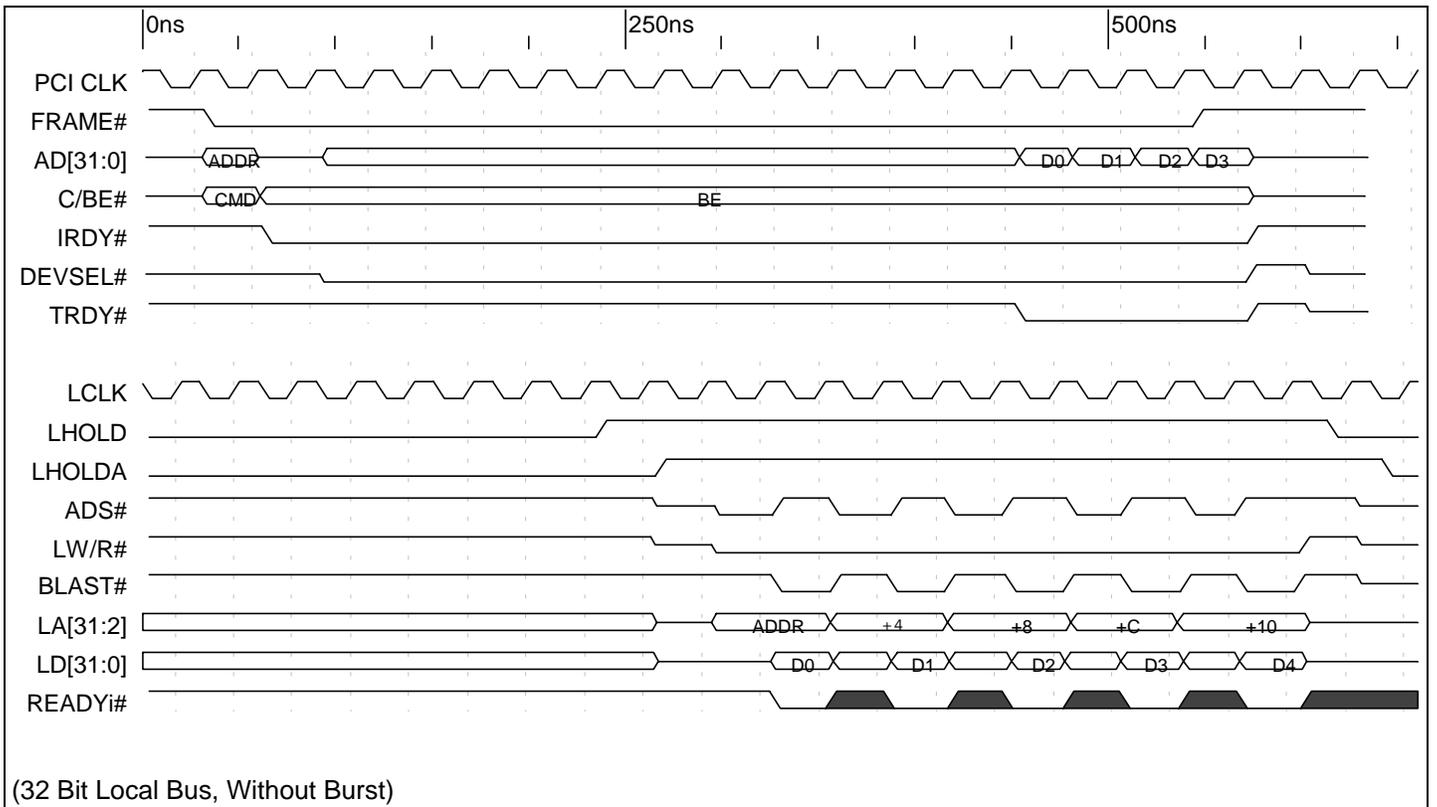
Timing Diagram 8-11. (Cx Mode) PCI 9060SD Direct Slave Single Cycle Read

Unused read data is flushed.

Bterm off, the local i960 only burst four at a time.
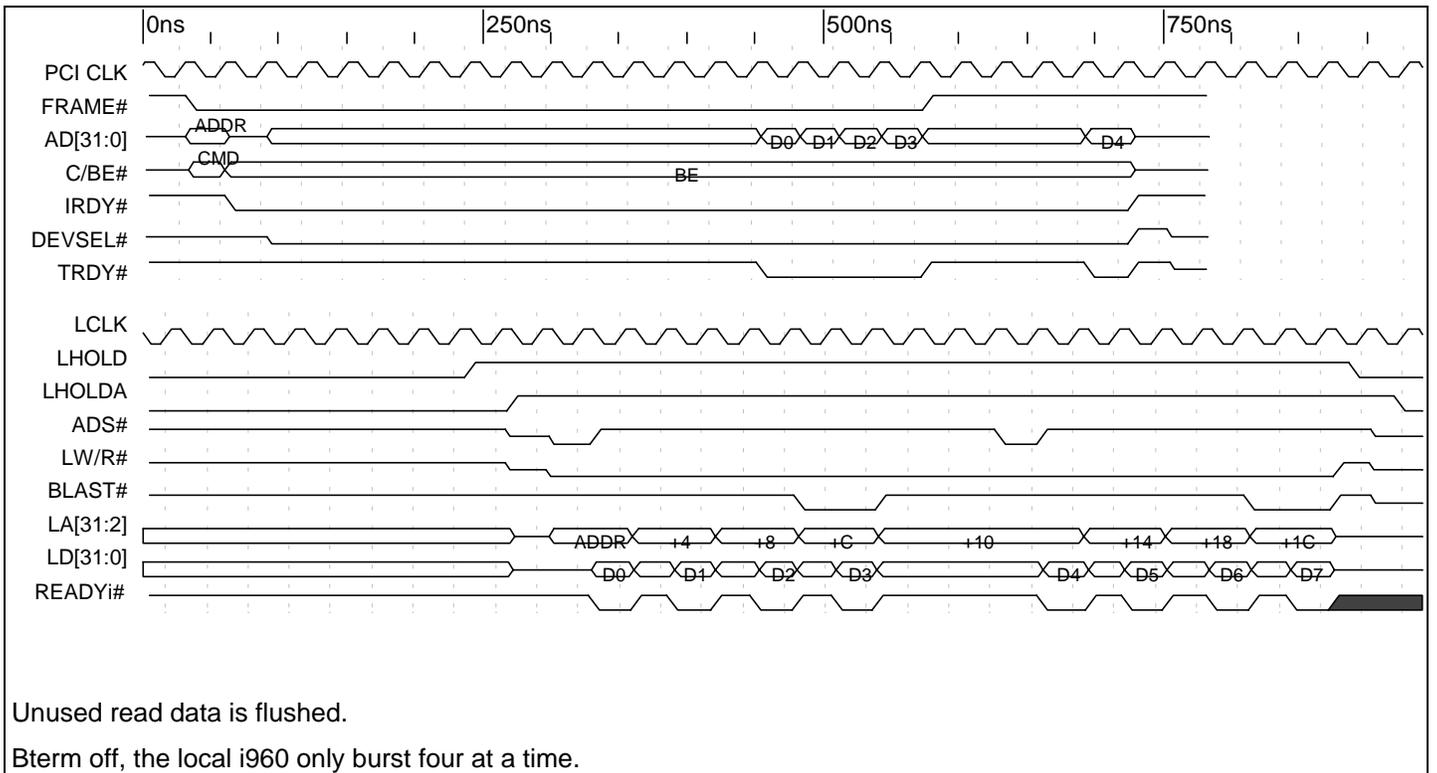
Timing Diagram 8-12. (Cx Mode) PCI 9060SD Direct Slave Burst Read of 5 Lwords (One Wait State)

(32 bit local bus, burst enabled, prefetch counter set to 5 Lwords)
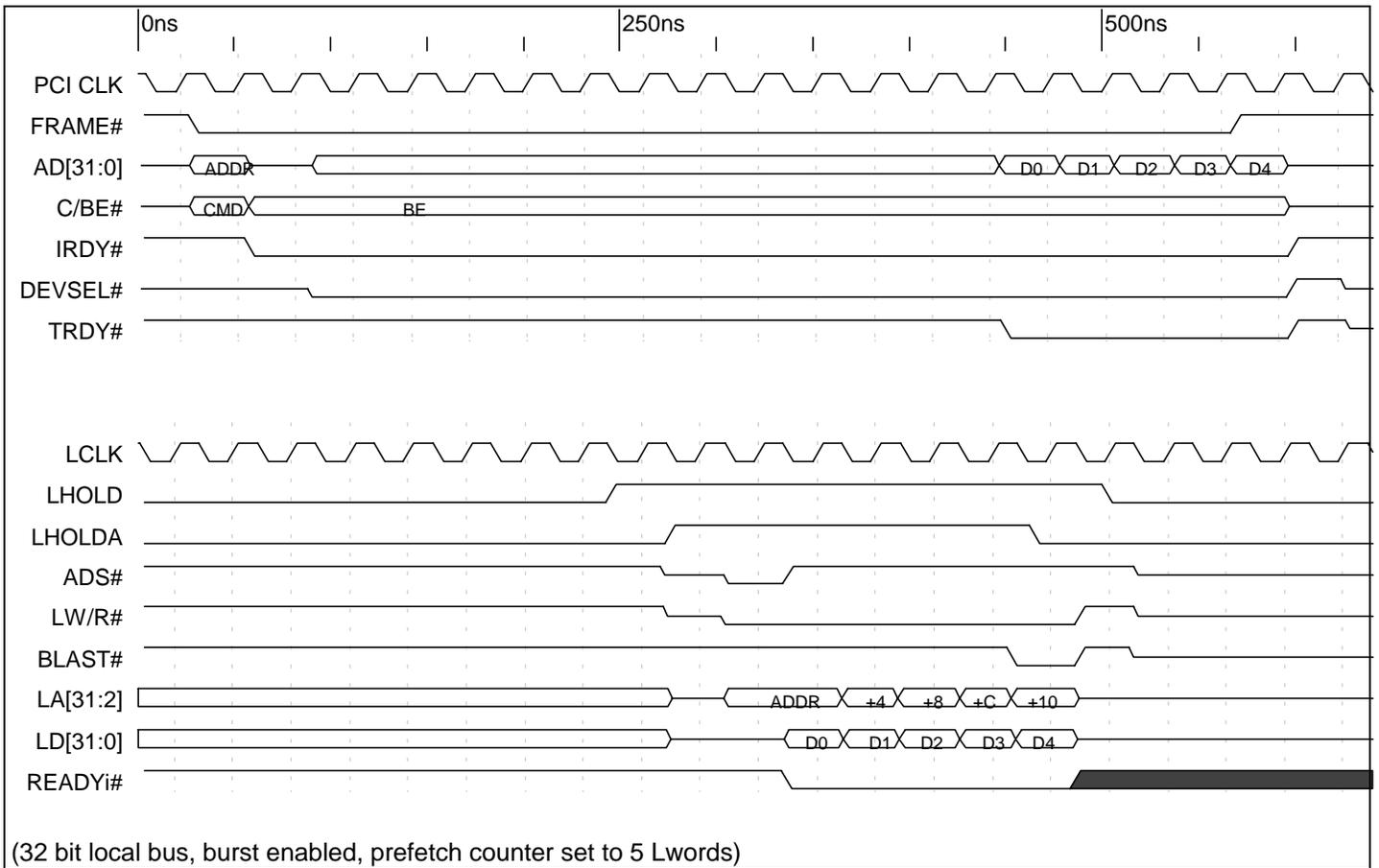
Timing Diagram 8-13. (Cx Mode) PCI 9060SD Direct Slave Burst Read with Prefetch Counter Set to 5
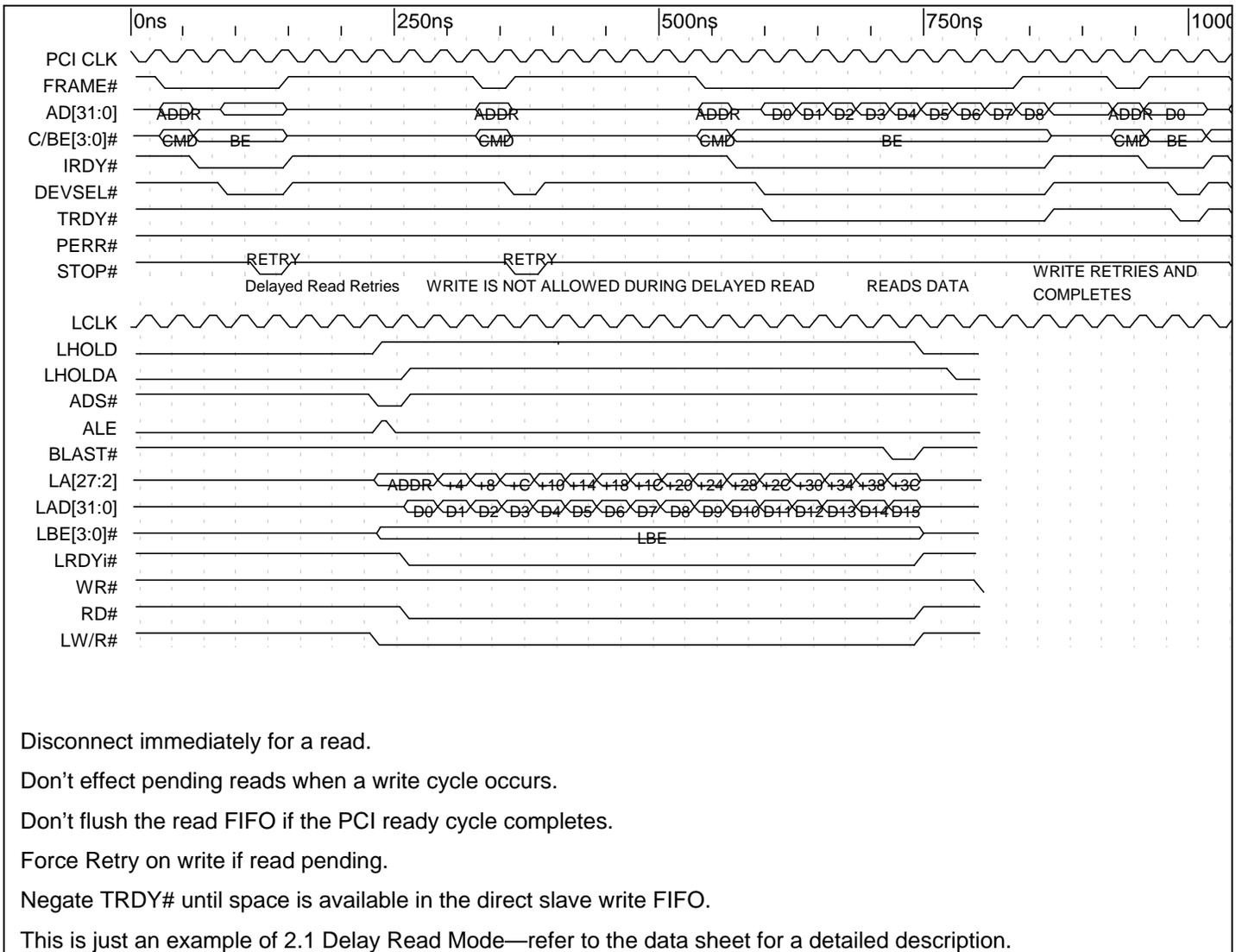
Disconnect immediately for a read.

Don't effect pending reads when a write cycle occurs.

Don't flush the read FIFO if the PCI ready cycle completes.

Force Retry on write if read pending.

Negate TRDY# until space is available in the direct slave write FIFO.

This is just an example of 2.1 Delay Read Mode—refer to the data sheet for a detailed description.

Timing Diagram 8-14. (Cx Mode) PCI 9060SD Direct Slave Read 2.1 Mode

(No wait states, 32-bit bus, burst enabled)
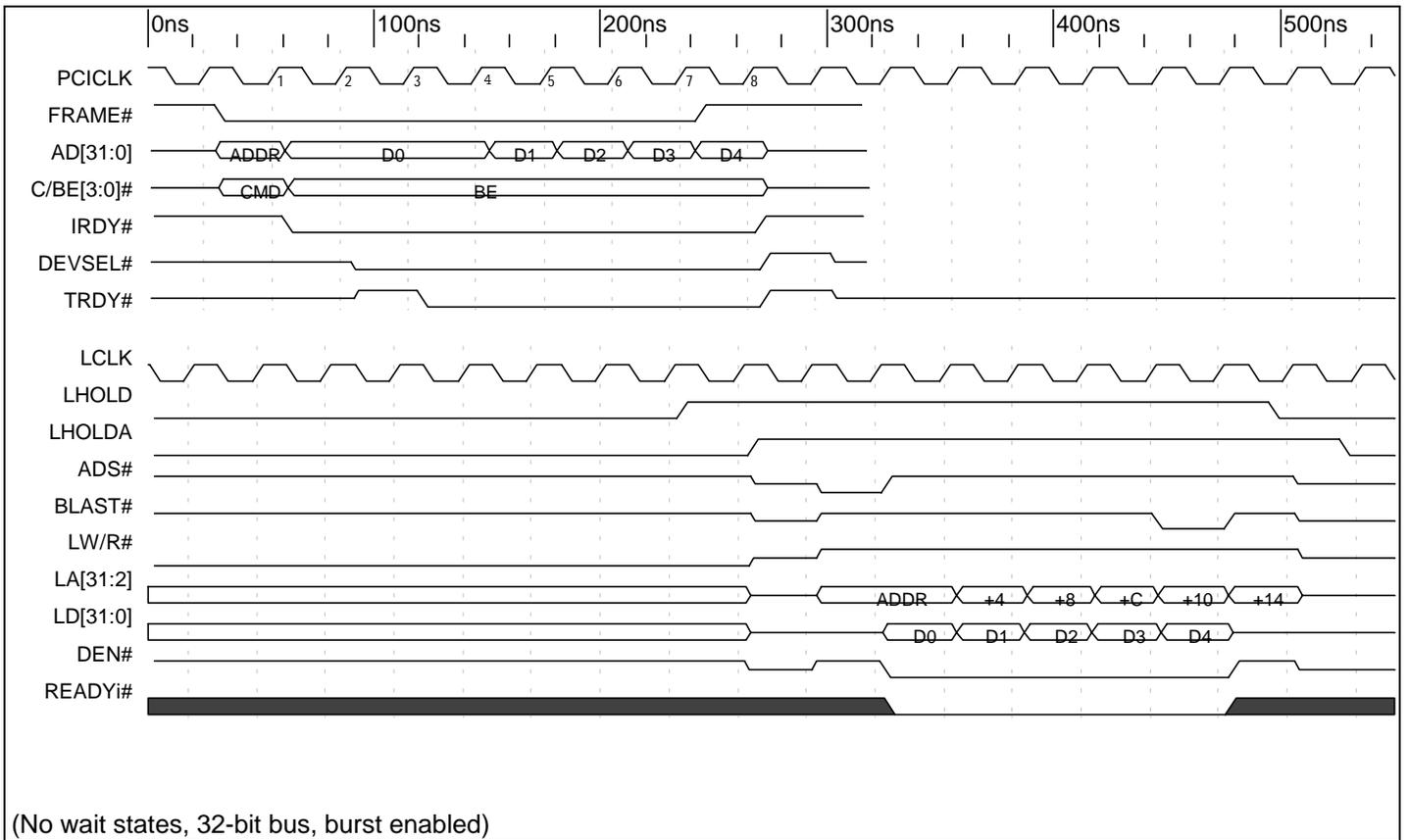
Timing Diagram 8-15. (Cx Mode) PCI 9060SD Direct Slave PCI to Local Burst Write

(1 wait state, 32-bit bus, burst enabled)
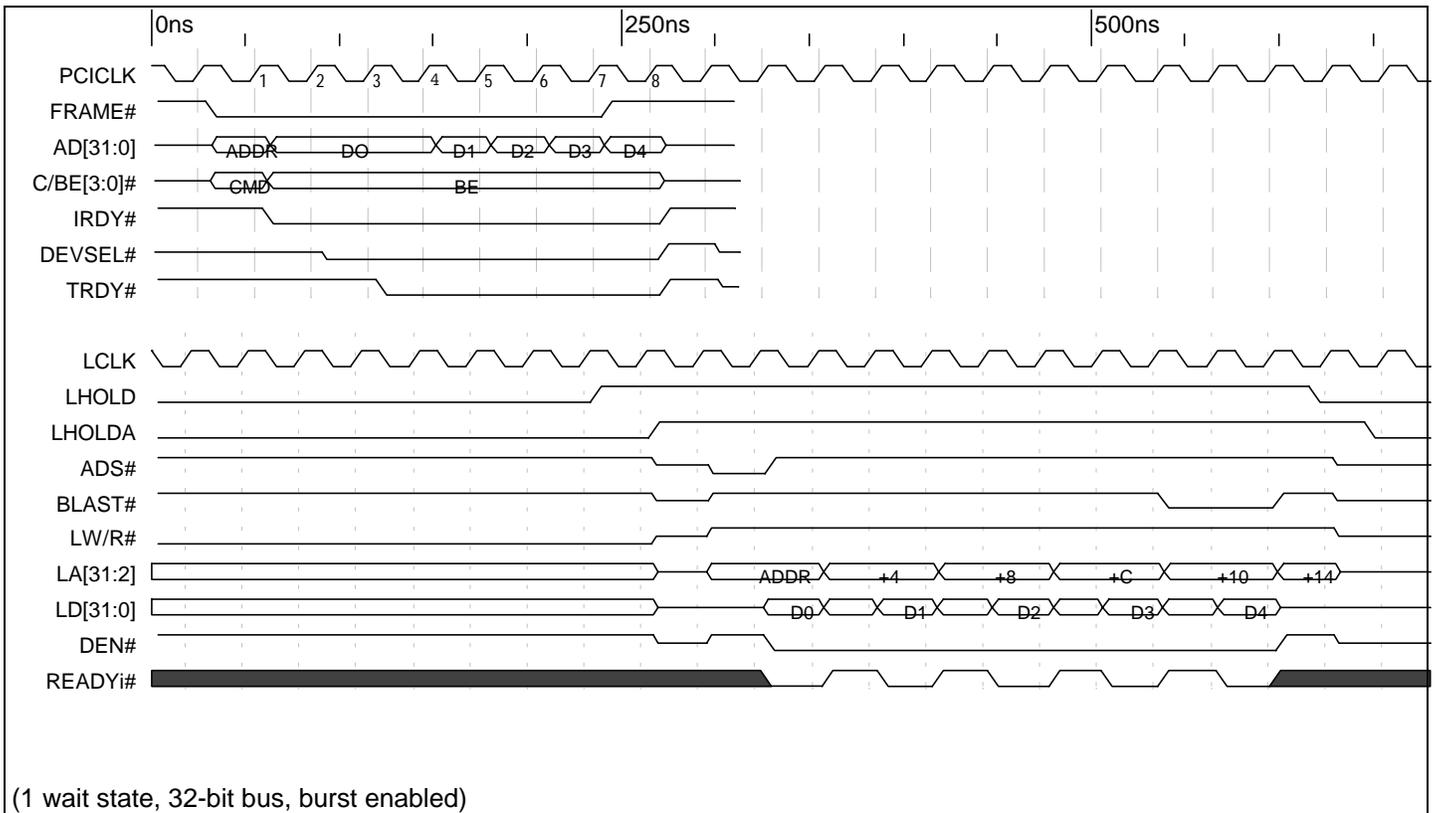
Timing Diagram 8-16. (Cx Mode) PCI 9060SD Direct Slave PCI to Local Burst Write (One Wait State)

	0ns					250ns					500ns			

LCLK

LHOLD — <--- PCI 9060SD DRIVES BUS — PCI 9060SD FLOATS BUS -->

LHOLDA

ADS#

BLAST#

LBE[3:0]# — 0000, DOES NOT CHG, UNALIGNED HAS OWN CYCLE WITH ADS

LW/R#

LD[31:0] — D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10

LA[31:2] — A A+4 A+8 A+C A+10 A+14 A+18 A+1C A+20 A+24 A+28

DT/R#

DEN#

BTERM# — BTERM FORCES NEW ADS# -->

READYi#

Note: BTERM# is a ready input which also causes a new ADS# cycle.
Note: not all byte enables asserted will cause a new ADS# cycle.
(No wait states, 32-bit bus, burst enabled, Bterm enabled)

Timing Diagram 8-17. (Cx Mode) PCI 9060SD DMA or Direct Slave Burst Write, Bterm Enabled

Note: Not all byte enables asserted or a quad boundary LA[3:2]=11 results in a new ADS#.

(No wait states, 32-bit bus, burst enabled, Bterm disabled, the local i960 only burst four at a time).
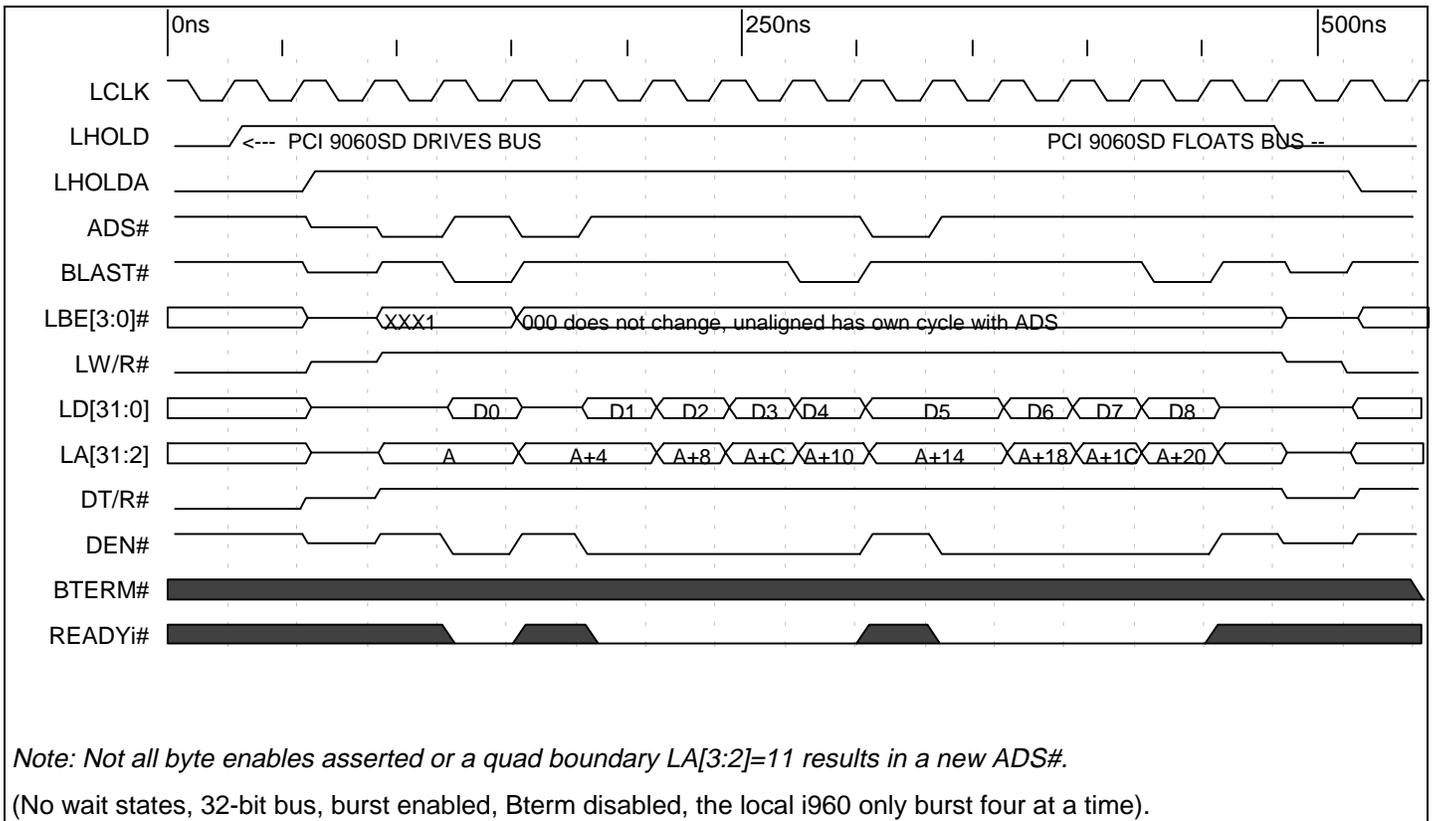
Timing Diagram 8-18. (Cx Mode) PCI 9060SD DMA or Direct Slave Burst Write, Bterm Disabled

(No wait states, 8 bit bus, burst enabled)
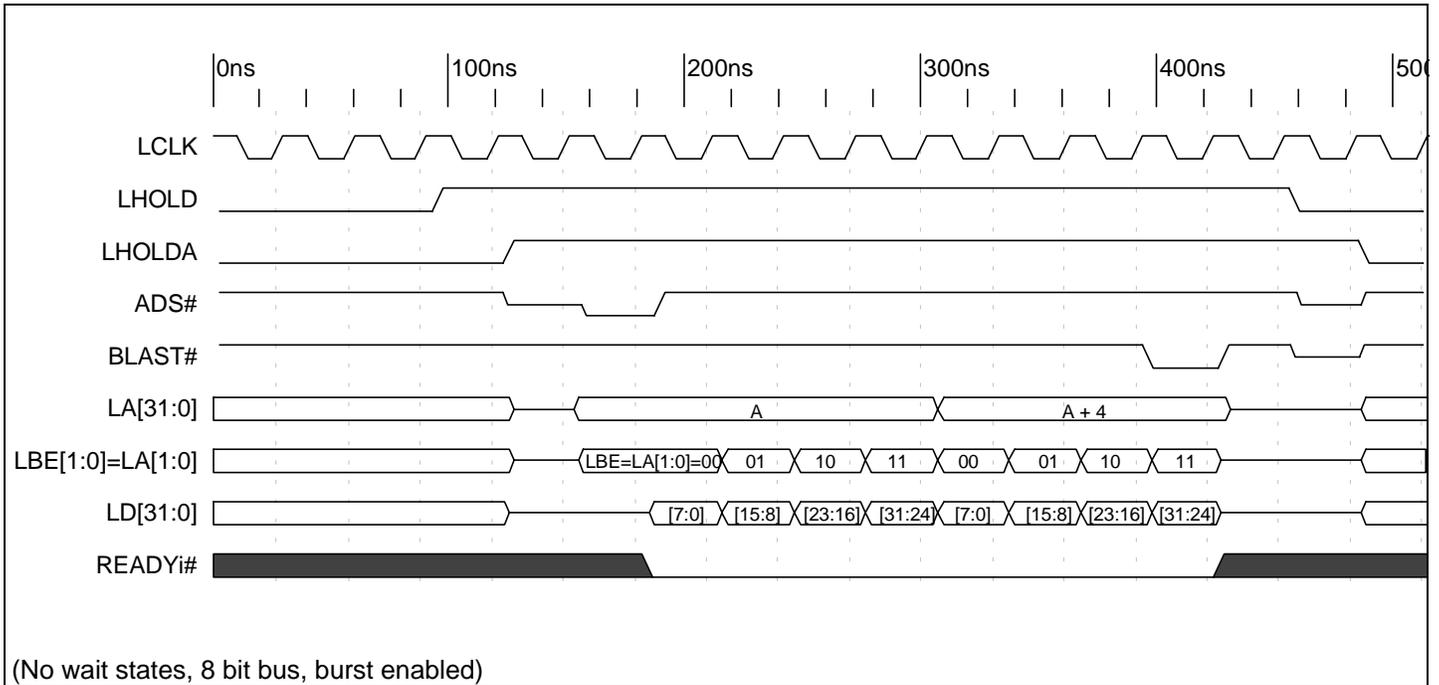
Timing Diagram 8-19. (Cx Mode) DMA or Direct Slave 2 Lword Burst Write to 8 Bit Local Bus

(No wait states, 16 bit bus, burst enabled)
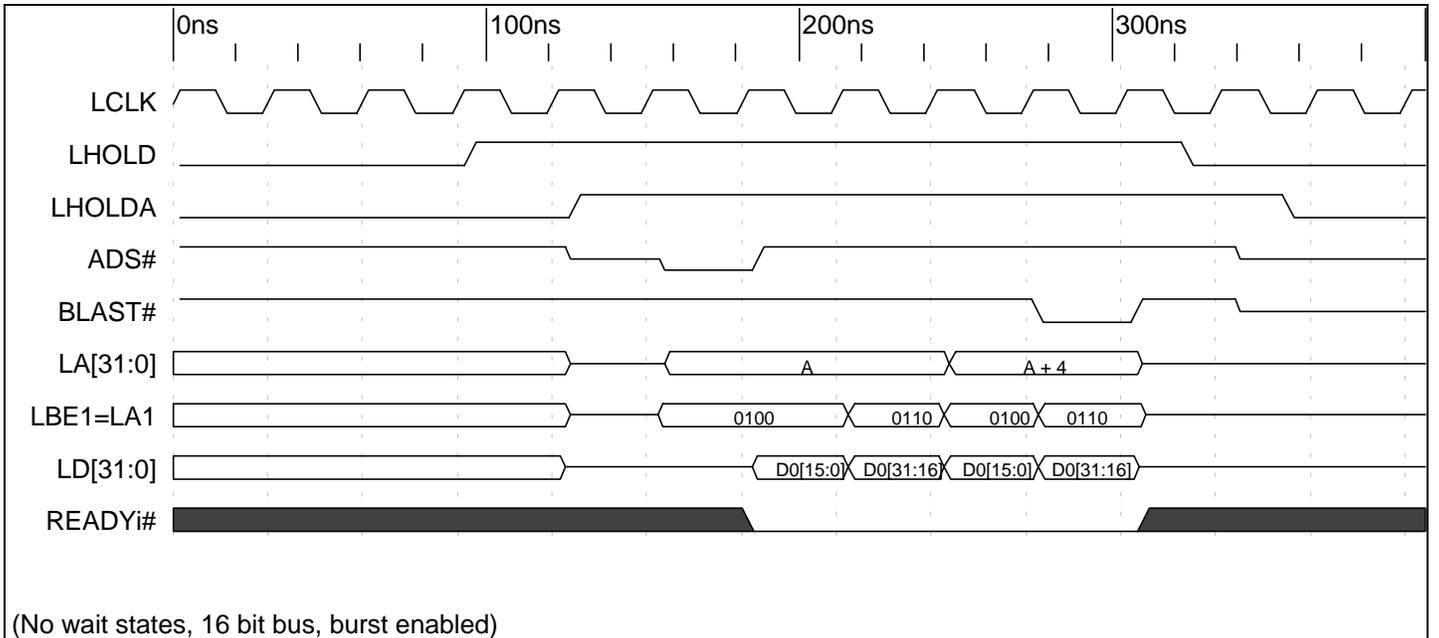
Timing Diagram 8-20. (Cx Mode) DMA or Direct Slave 2 Lword Burst Write to 16 Bit Local Bus

(No wait states, 32 bit local bus)
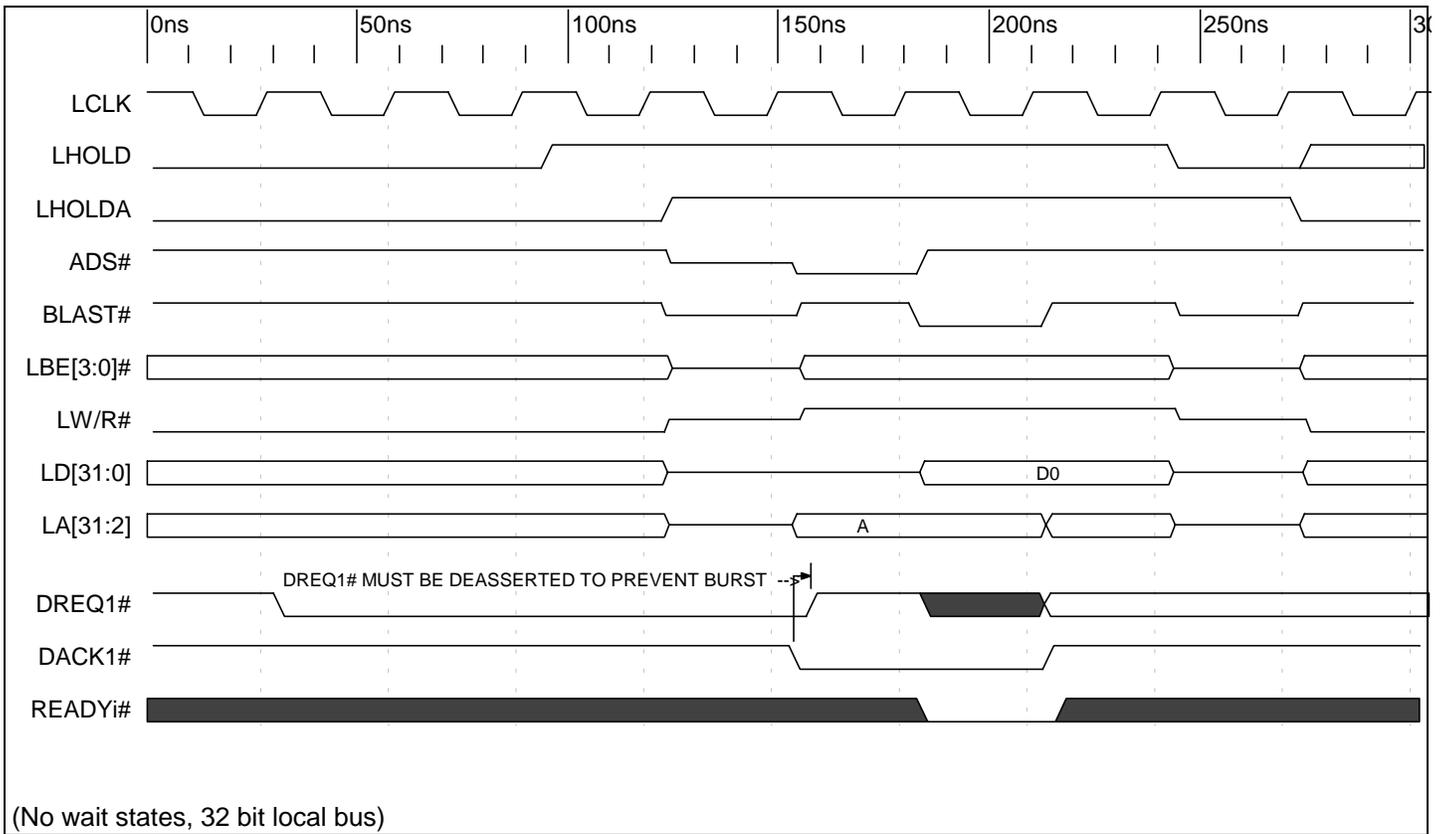
Timing Diagram 8-21. (Cx Mode) Single Cycle DMA Demand Mode PCI to Local

(No wait states, burst enabled, Bterm enabled, 32 bit local bus)
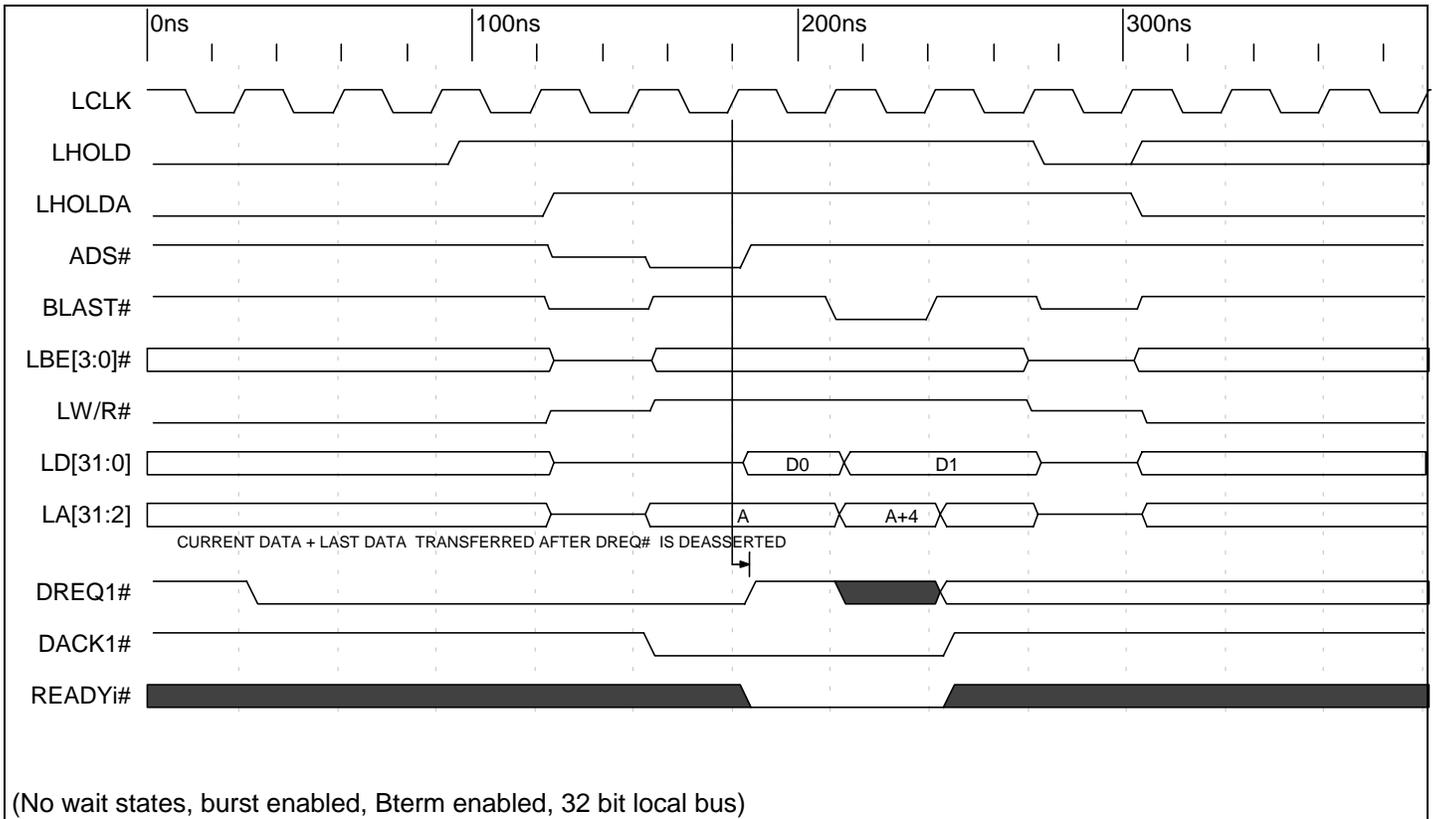
Timing Diagram 8-22. (Cx Mode) Multiple Cycle DMA Demand Mode PCI to Local

(No wait states, 32-bit bus)

First Address A are bits [31:4] of the next descriptors pointer register.

D0: PCI Start Address, D1: Local Start Address, D2: Transfer Count (bytes), D3: Next Descriptor Pointer.
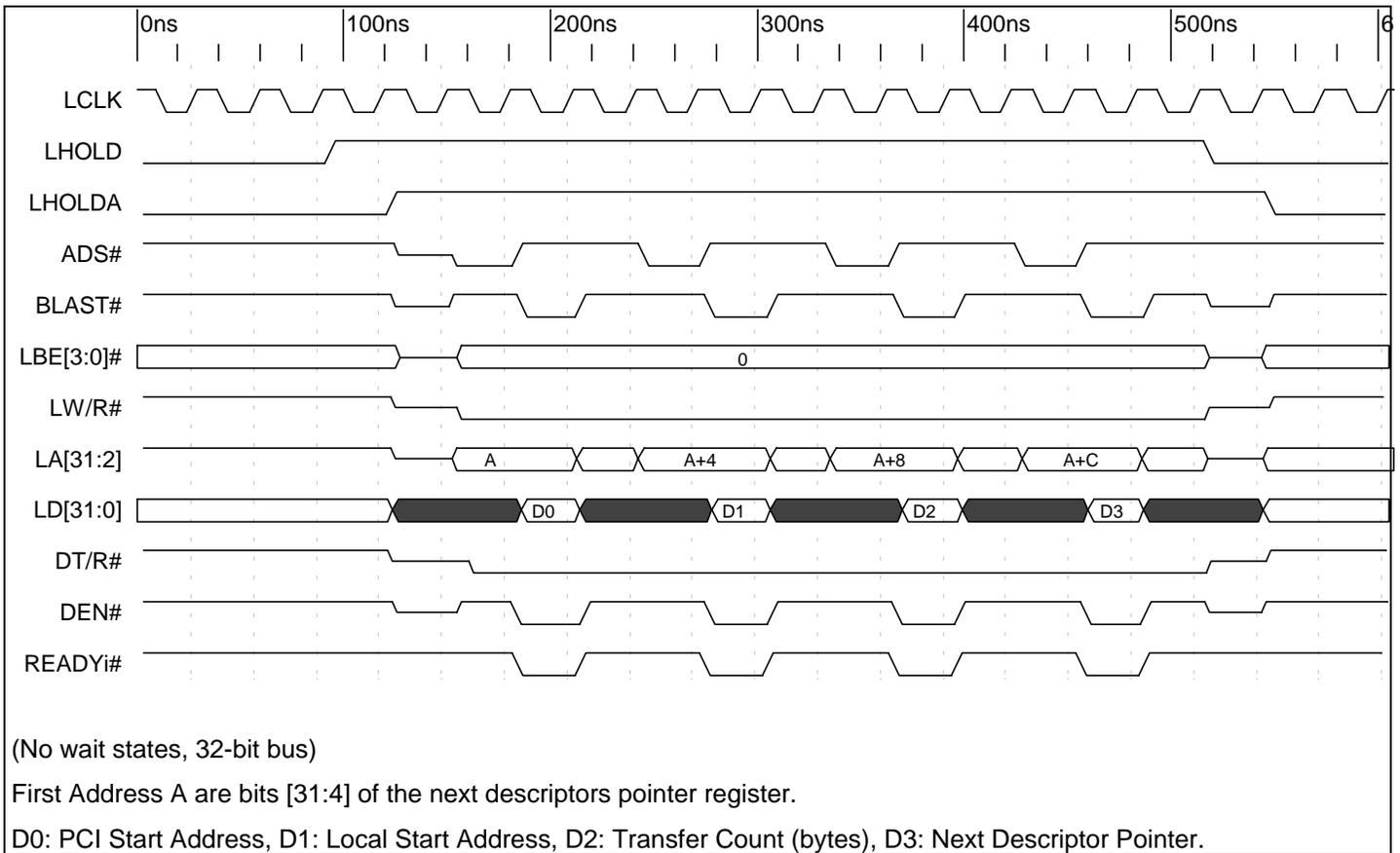
Timing Diagram 8-23. (Cx Mode) PCI 9060SD Read of DMA Chaining Parameters from Local Memory

(No wait states, 32 bit local bus)

The Stop Data Transfer Mode bit is not set.

Refer to Table 4-43 for DMA Channel 1 Mode Register (LOC 114h) (PCI 94h), bit 15.
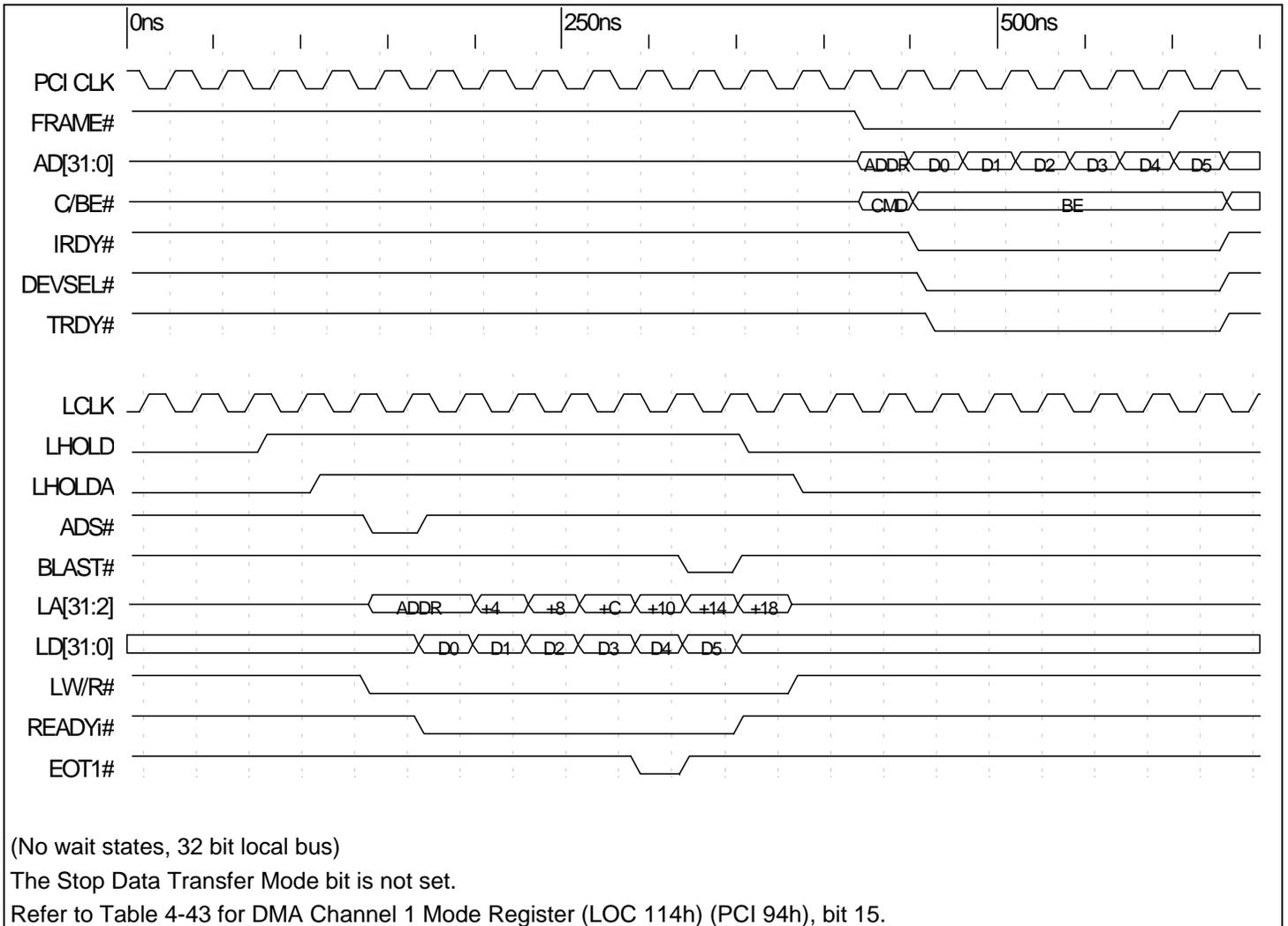
Timing Diagram 8-24. (Cx Mode) PCI 9060SD DMA Local to PCI, EOT Enabled

| | 0ns | | | | | | 250ns | | | | | 500ns | | |

PCI CLK

FRAME#

AD[31:0] — ADDR — D0 — D1 — D2 — D3 — D4 — D5 — D6 — D7

C/BE# — CMD — BE

IRDY#

DEVSEL#

TRDY#

LCLK

LHOLD

LHOLDA

ADS#

BLAST#

LA[31:2] — ADDR — +4 — +8

LD[31:0] — D0 — D1

LW/R#

READYi#

EOT1#

(No wait states, 32 bit local bus)

The Stop Data Transfer Mode bit is not set.

Refer to Table 4-43 for DMA Channel 1 Mode Register (LOC 114h) (PCI 94h), bit 15.
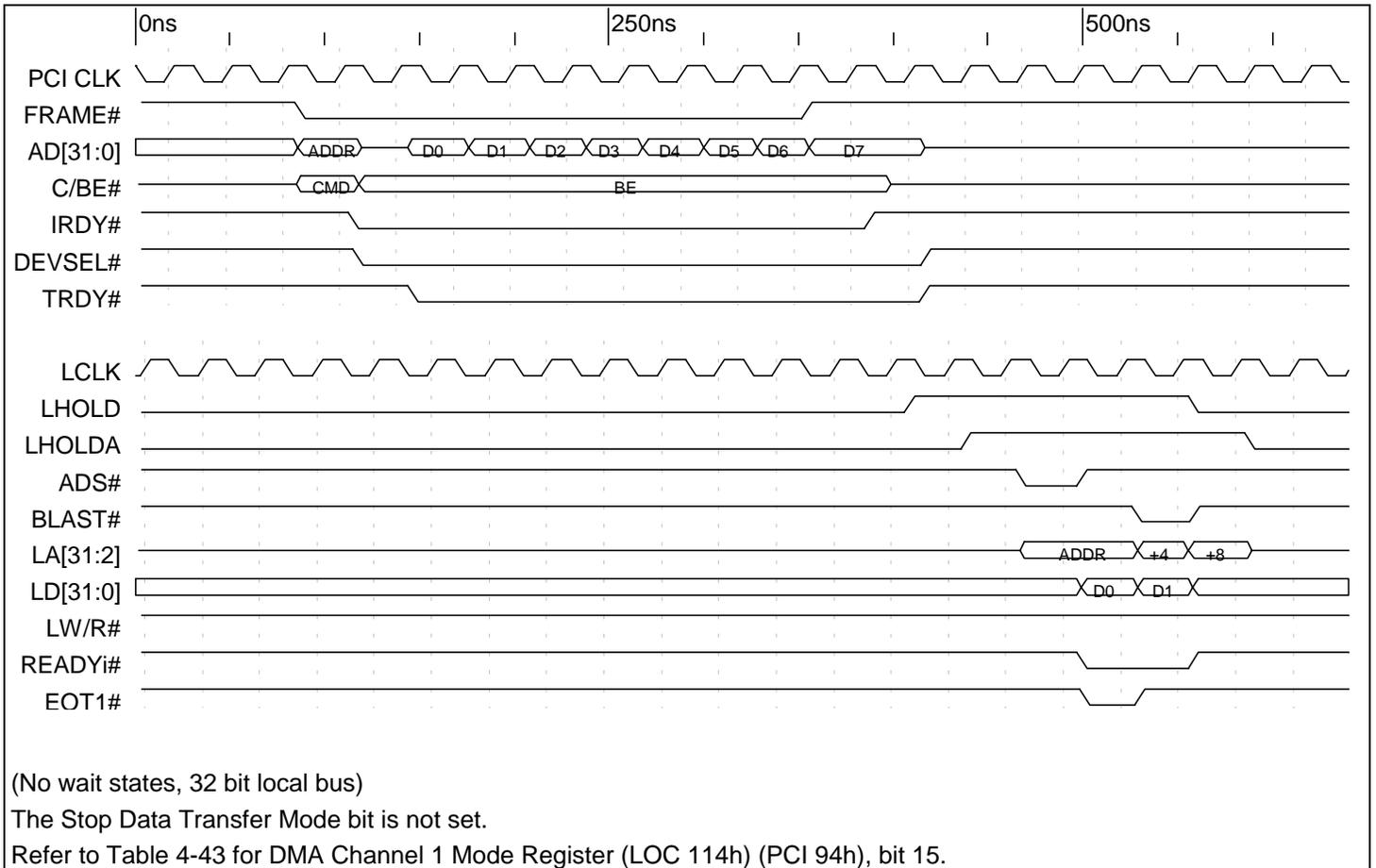
Timing Diagram 8-25. (Cx Mode) PCI 9060SD DMA PCI to Local, EOT Enabled

Latency Timer = 7 CLKs, Pause Timer = 4 CLKs. The PCI 9060SD internally adds another clock to the pause timer.
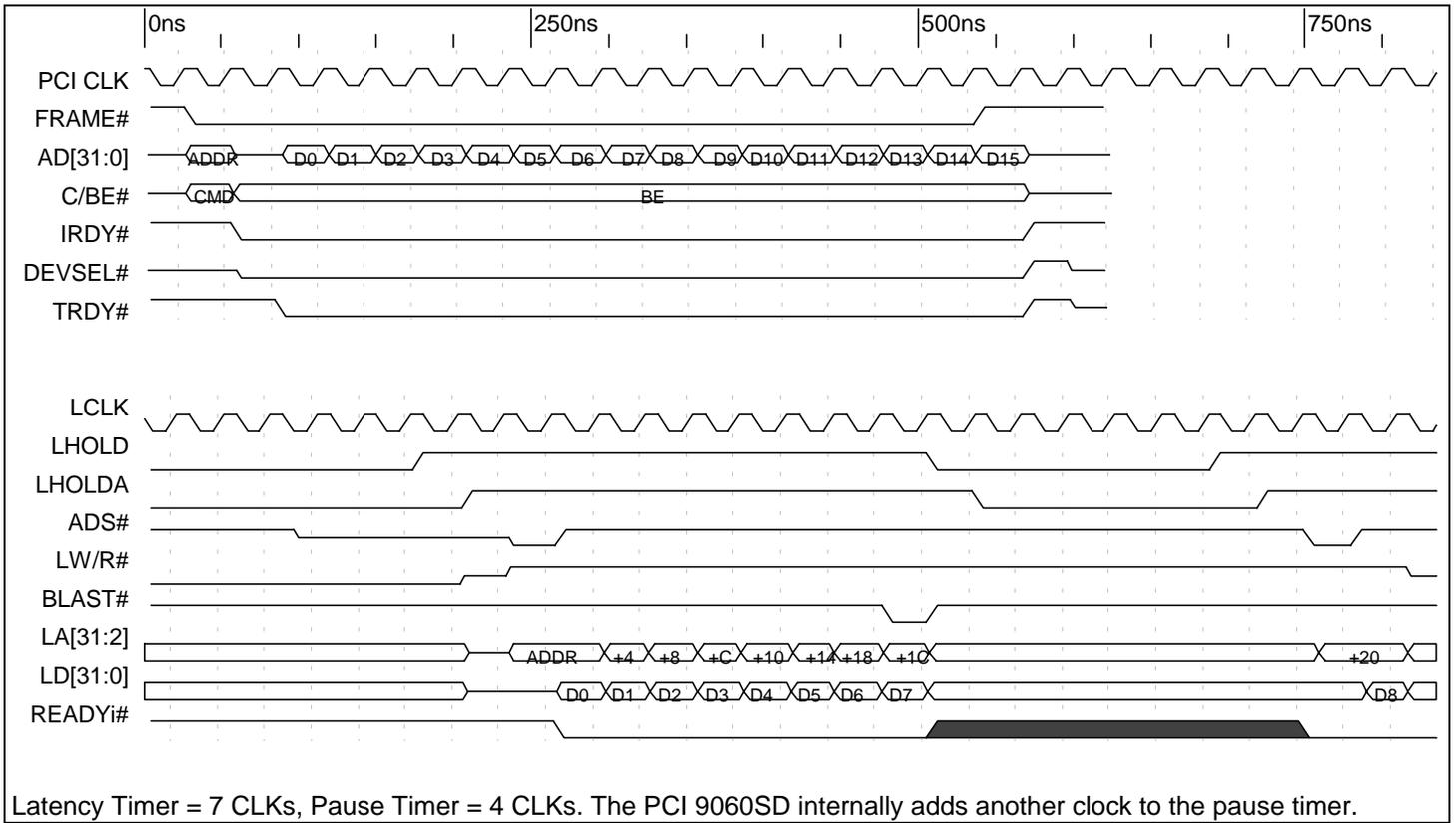
Timing Diagram 8-26. (Cx Mode) PCI 9060SD DMA PCI to Local with Local Pause Timer and Local Latency Timer
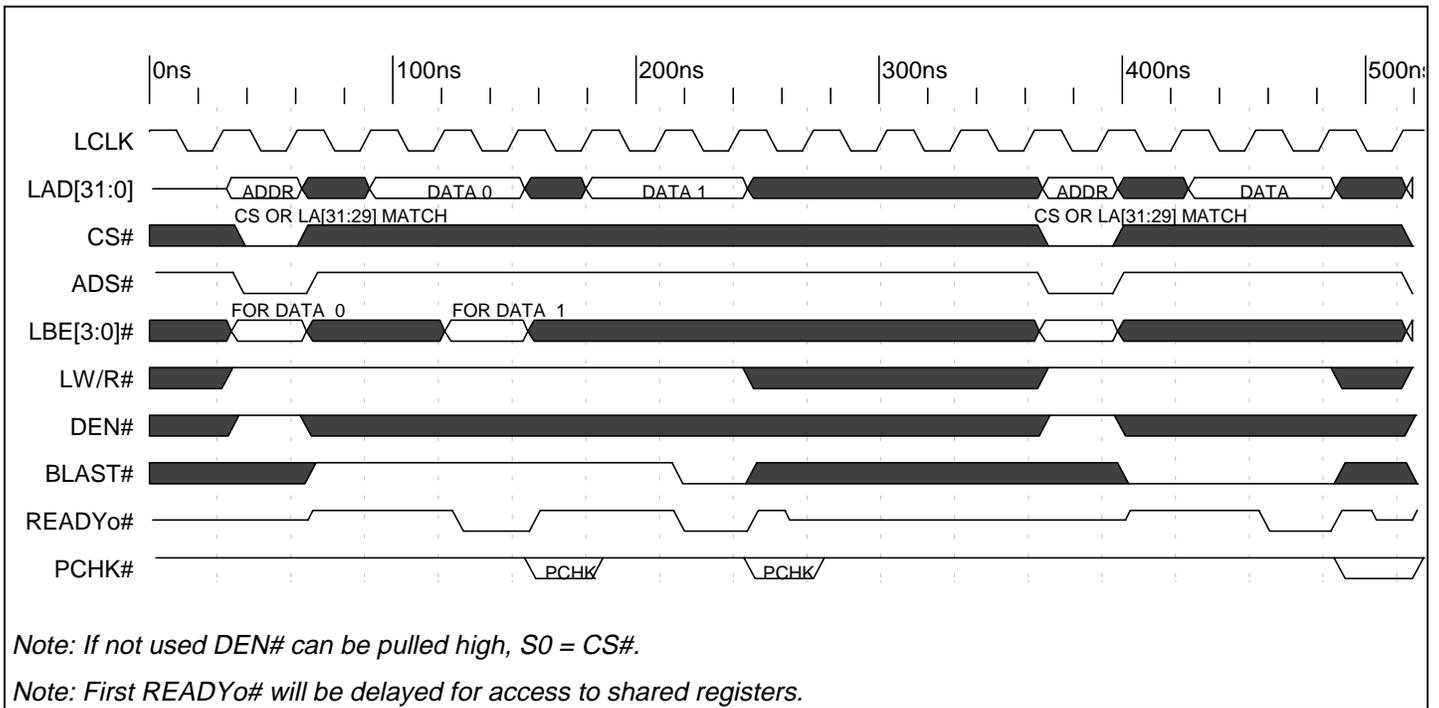
Timing Diagram 8-27. (Jx Mode) Local Bus Write to PCI 9060SD Configuration Register

Note: If not used DEN# can be pulled high, S0 = CS#.

Note: First READYo# will be delayed for access to shared registers.
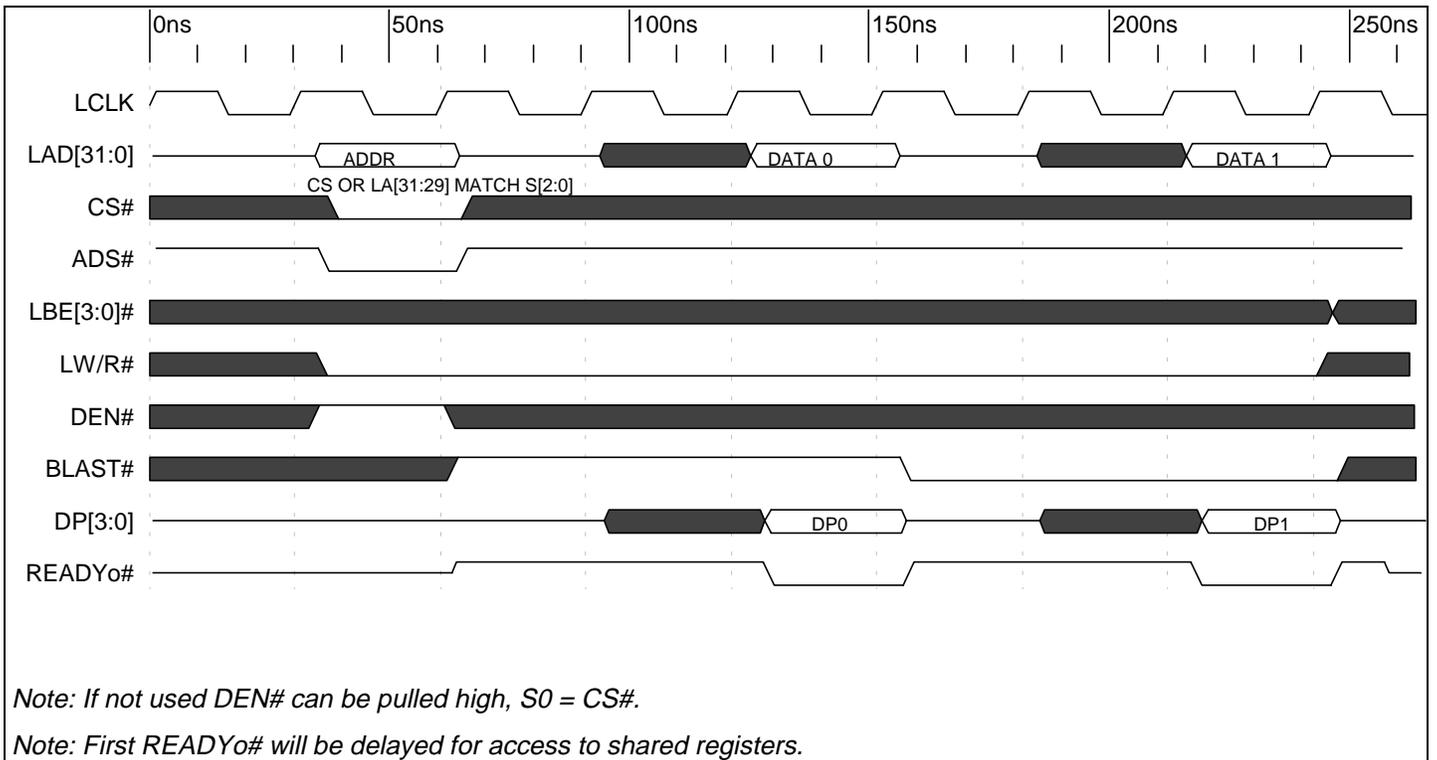
Timing Diagram 8-28. (Jx Mode) Local Bus Read from PCI 9060SD Configuration Register

Note: BTERM# is a ready input which also causes a new ADS# cycle.

(No wait states, 32-bit bus, burst enabled)
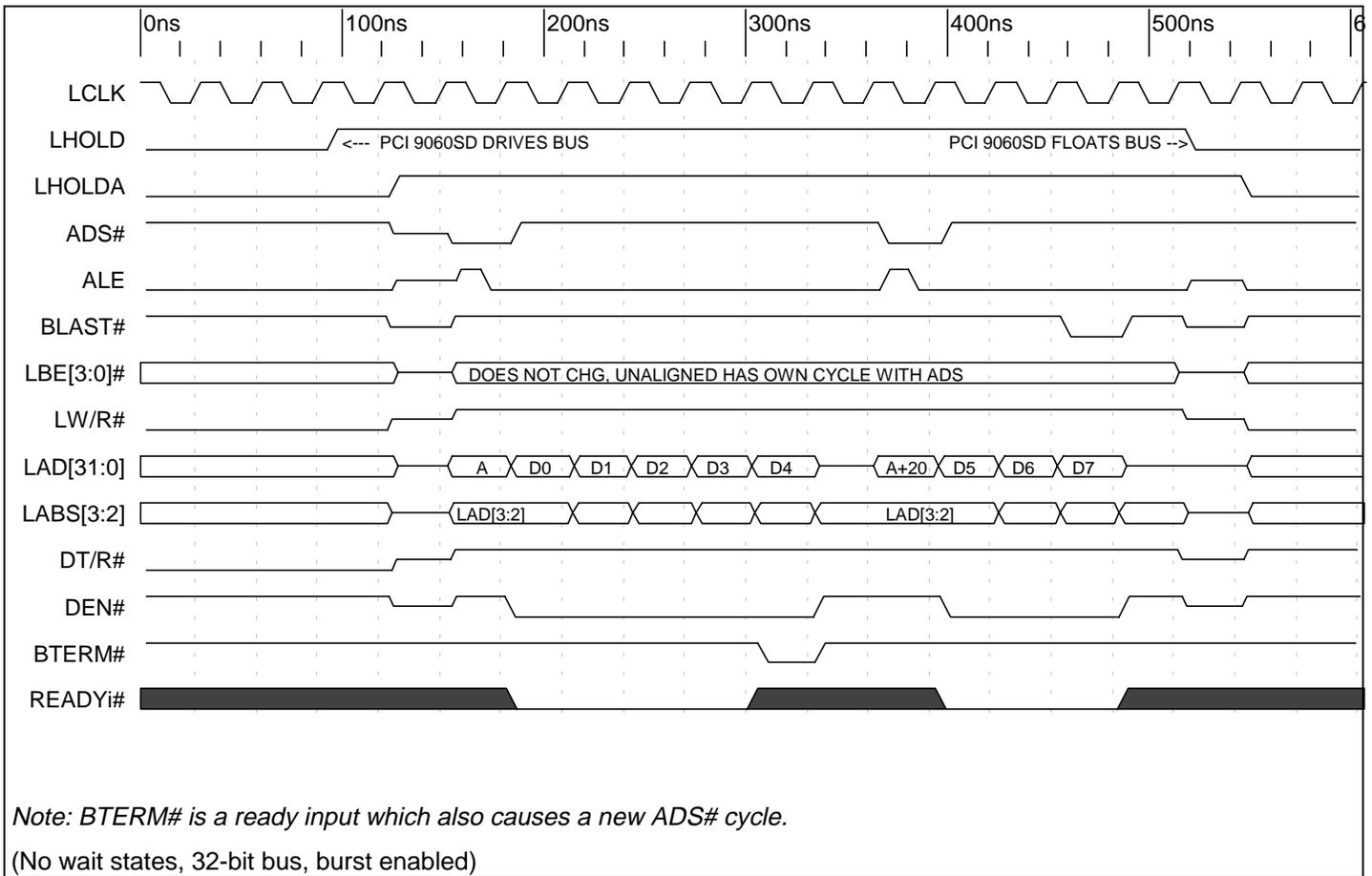
Timing Diagram 8-29. (Jx Mode) DMA or Direct Slave Burst Write, Bterm Enabled

Note: When Bterm is disabled, a new ADS (address) cycle starts every quad word boundary.

(No wait states, 32-bit bus, burst enabled)
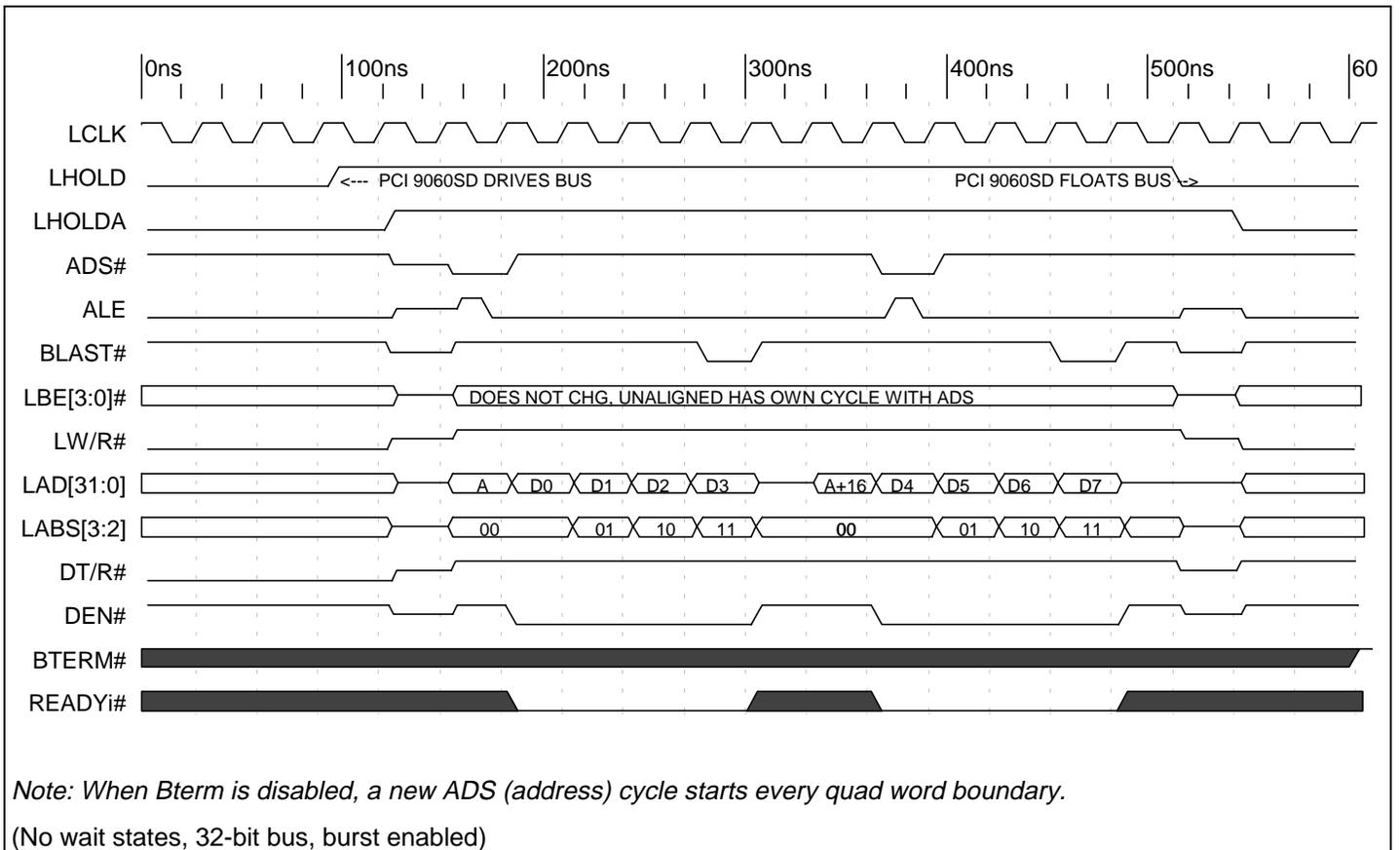
Timing Diagram 8-30. (Jx Mode) DMA or Direct Slave Burst Write, Bterm Disabled

	0ns	100ns	200ns	300ns	400ns	500ns	6
LCLK							
LHOLD		<--- PCI 9060SD DRIVES BUS			PCI 9060SD FLOATS BUS -->		
LHOLDA							
ADS#							
ALE							
BLAST#							
LBE[3:0]#			DOES NOT CHG, UNALIGNED HAS OWN CYCLE WITH ADS				
LW/R#							
LAD[31:0]		A	D0 D1 D2 D3 D4	A+20	D5 D6 D7		
LABS[3:2]		00	01 10 11 00 01		10 11		
DT/R#							
DEN#							
BTERM#							
READYi#							

(No wait states, 32-bit bus, burst enabled, Bterm enabled)
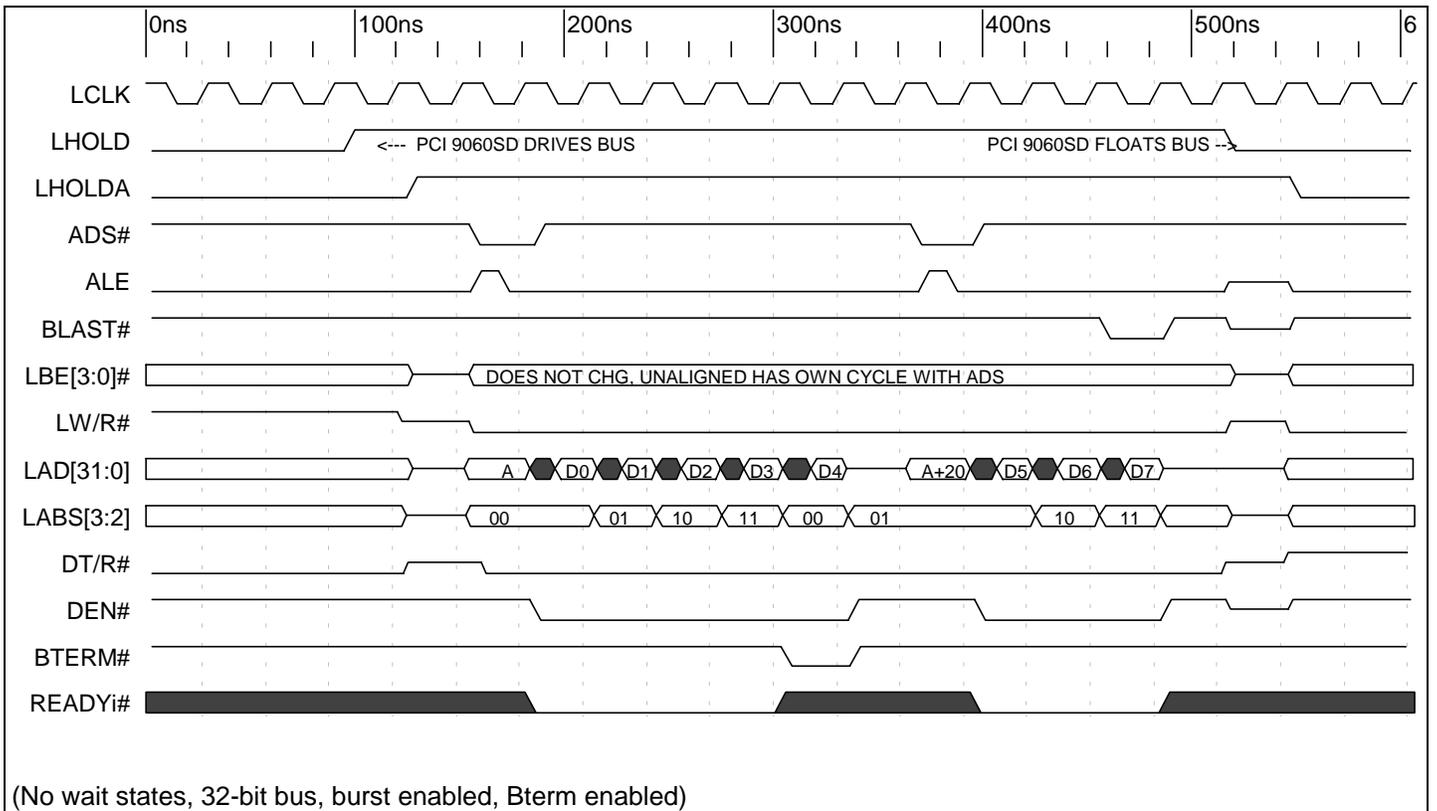
Timing Diagram 8-31. (Jx Mode) DMA or Direct Slave Burst Read, Bterm Enabled

	0ns				250ns				500ns				

LCLK

LHOLD   <--- PCI 9060SD DRIVES BUS   PCI 9060SD FLOATS BUS -->

LHOLDA

ADS#

ALE

BLAST#

LBE[3:0]#   DOES NOT CHG, UNALIGNED HAS OWN CYCLE WITH ADS

LW/R#

LAD[31:0]   A   D0   D1   D2   D3   D4   D5   D6   D7   D8   D9   A+28   D10

LABS[3:2]   LAD[3:2]

DT/R#

DEN#

BTERM#

READYi#

BREQ

OWNED BY i960   DMA CONTINUES
OR ANOTHER   WHERE IT LEFT
BUS MASTER OFF

(No wait states, 32-bit bus, burst enabled, Bterm enabled)
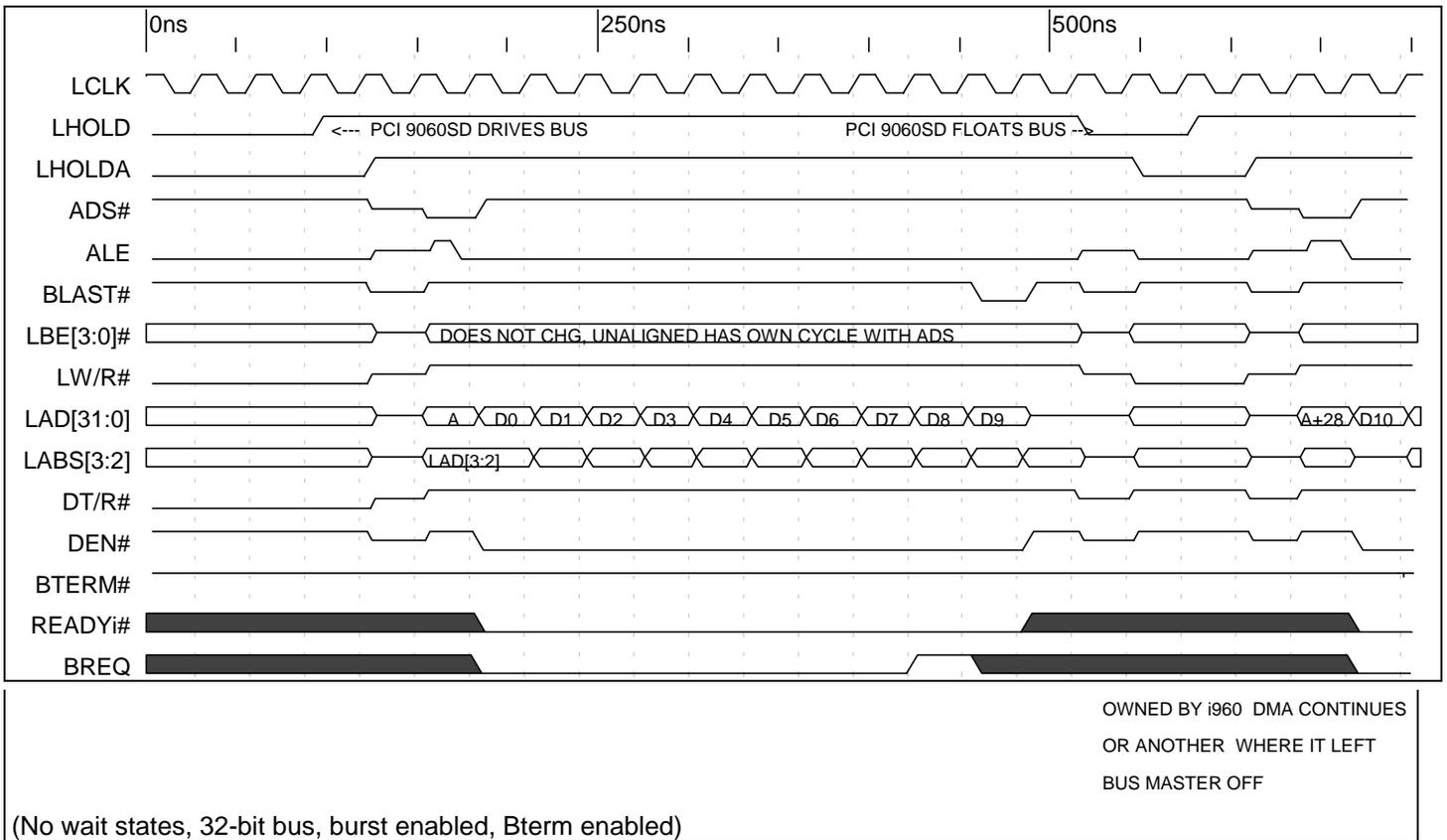
Timing Diagram 8-32. (Jx Mode) DMA Burst Write to 32 Bit Local Bus Suspended by BREQ Input

(No wait states, 32-bit bus)

First Address A are bits [31:4] of the next descriptors pointer register.

D0: PCI Start Address, D1: Local Start Address, D2: Transfer Count (bytes), D3: Next Descriptor Pointer.
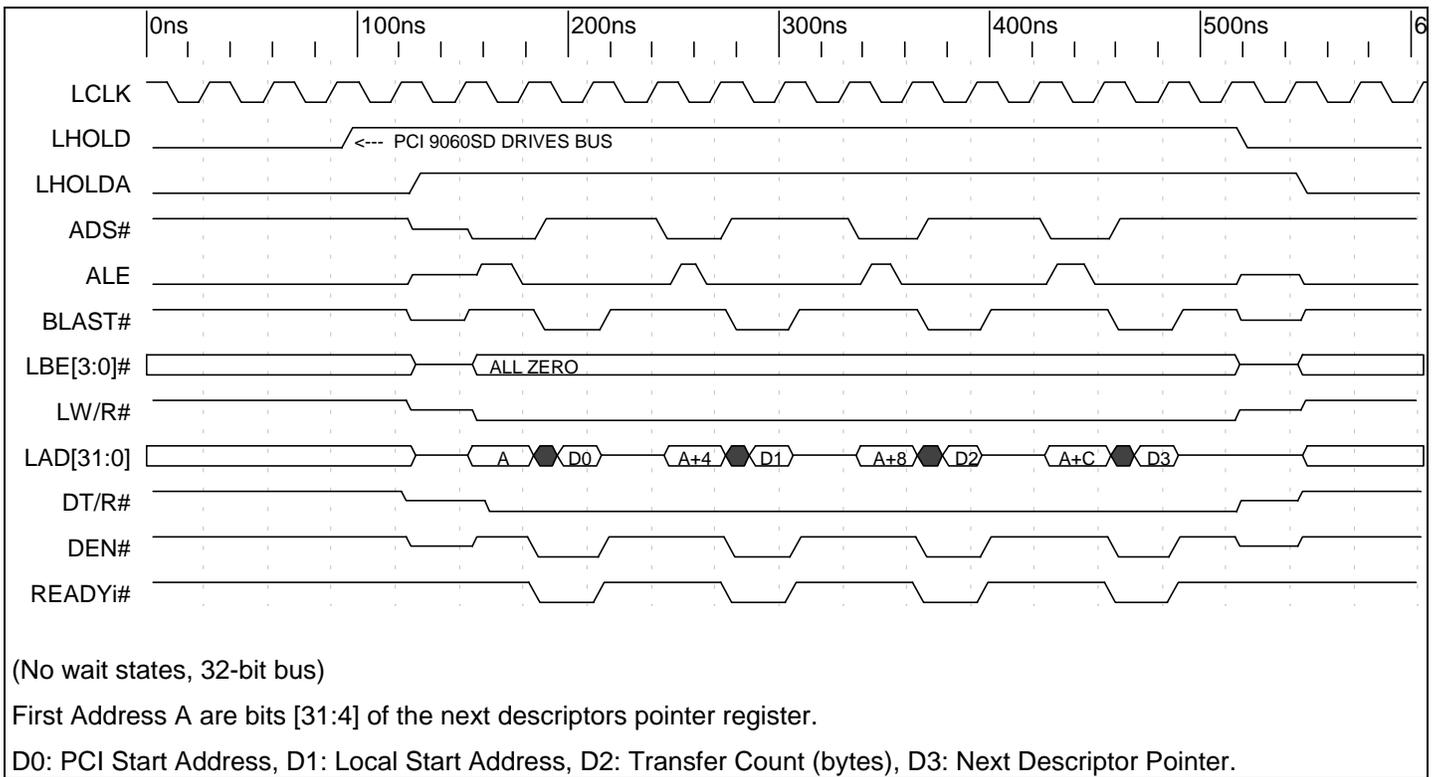
Timing Diagram 8-33. (Jx Mode) Read of DMA Chaining Parameters from Local Bus

LRESETo# must be used to establish phase A relationship as shown.
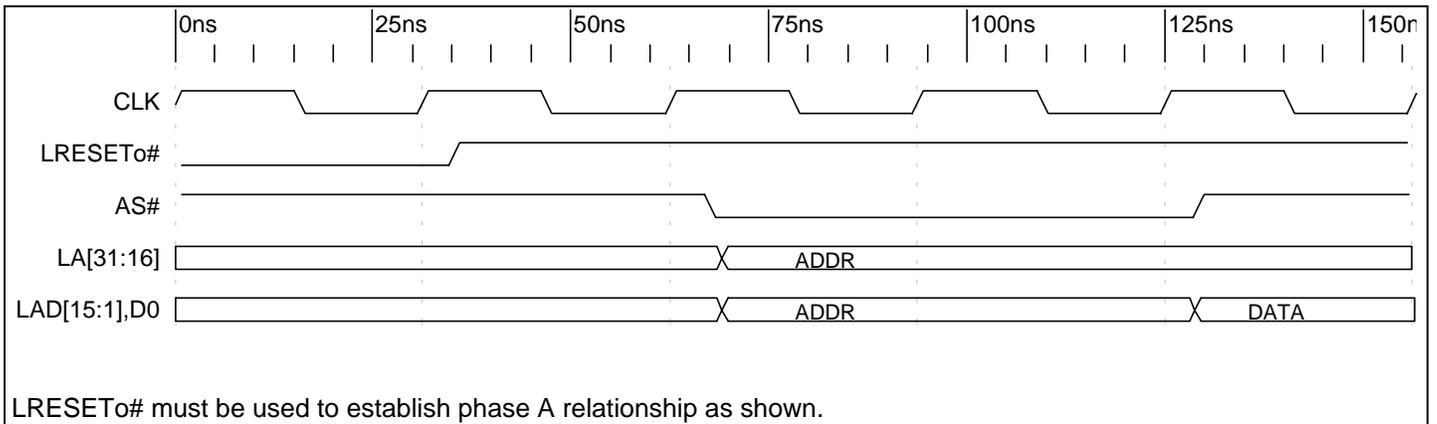
Timing Diagram 8-34. (Sx Mode) Two Phase Clock Synchronization Using LRESETo#
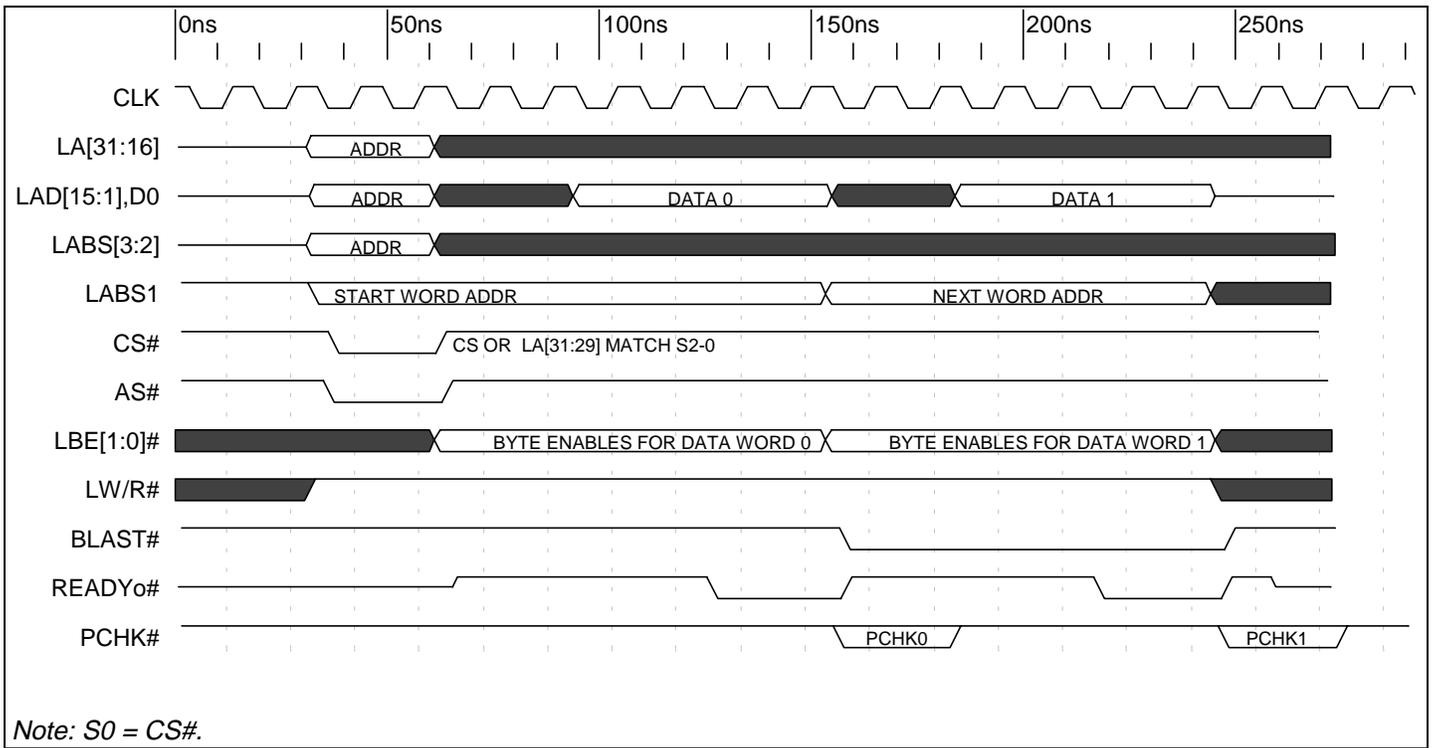
Timing Diagram 8-35. (Sx Mode) Local Bus Write to Configuration Register

Note: S0 = CS#.
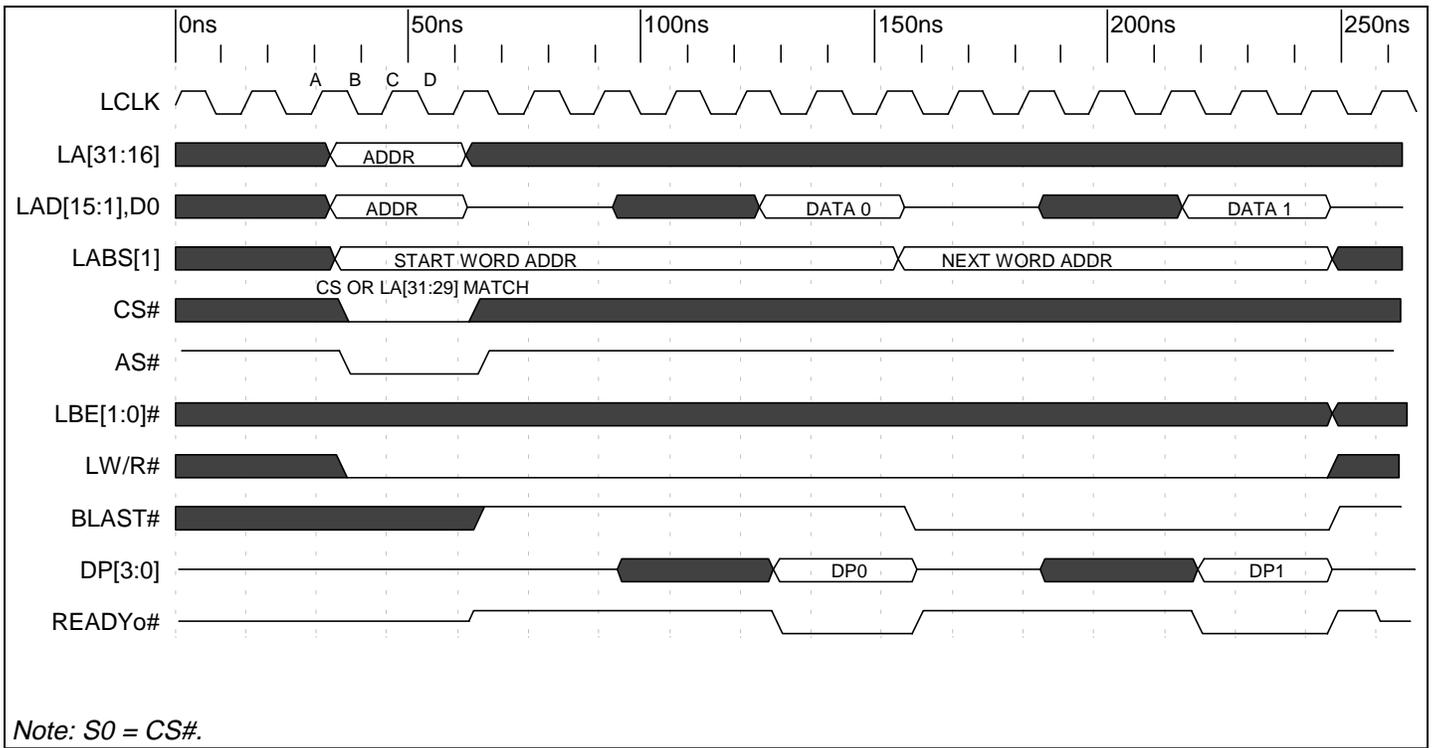
Timing Diagram 8-36. (Sx Mode) Local Bus Read from Configuration Register

	0ns	100ns	200ns	300ns	400ns	50C

LCLK

LHOLD

LHOLDA

ADS#

BLAST#

LA[31:16] A A+4 A + 8 A+C

LBE[1:0]#

LABS[3:1] A A+2 A+4 A+6 A+8 A+A A+C A+D

LAD[15:0],D0 A [15:0] [31:16] [15:0] [31:16] [15:0] [31:16] [15:0] [31:16]

BTERM#

READYi#

Note: Not all byte enables asserted results in a new AS#.

(No wait states, burst enabled, Bterm enabled)
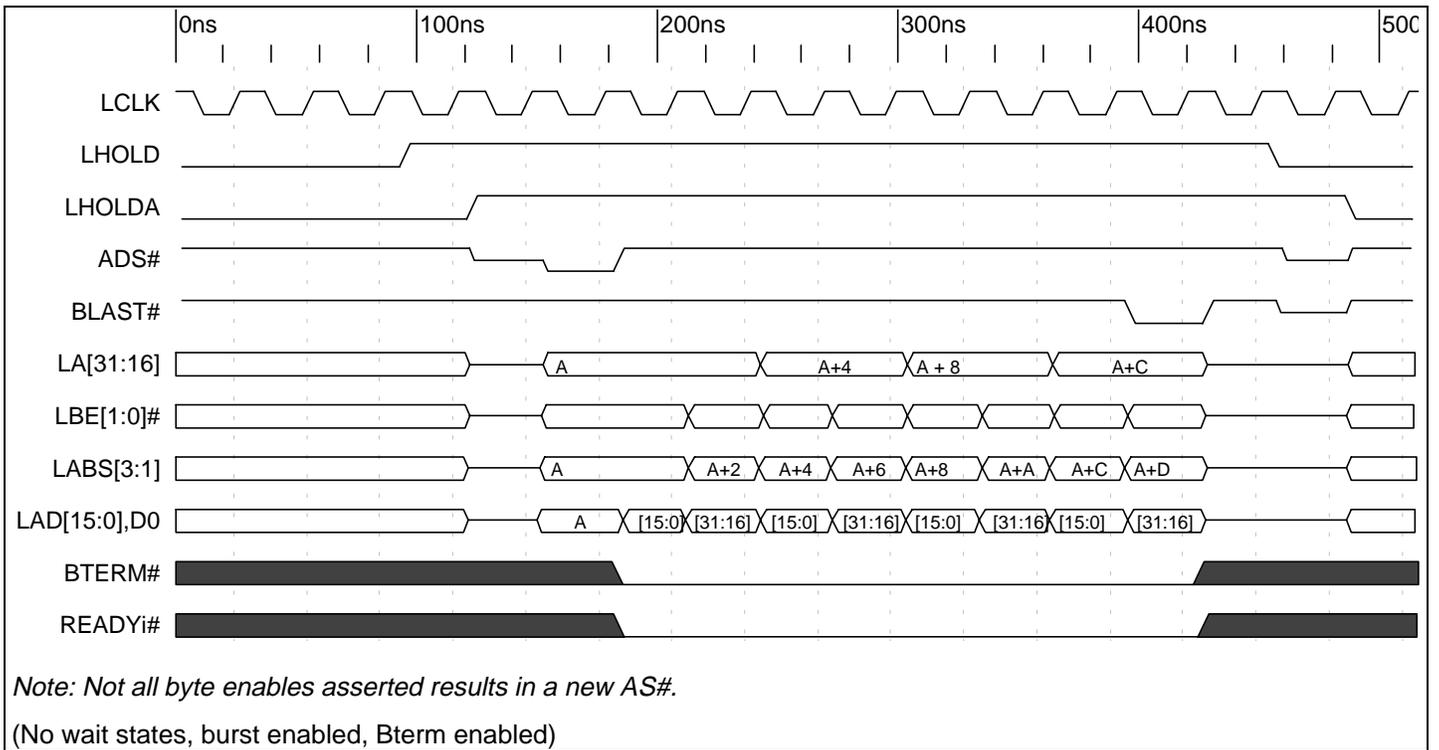
Timing Diagram 8-37. (Sx Mode) Direct Slave or DMA Burst Write to Local Bus